1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K75F MLB, "MEMSWAP"

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0000892544	PRODUCTION RELEASED	2010-04-15

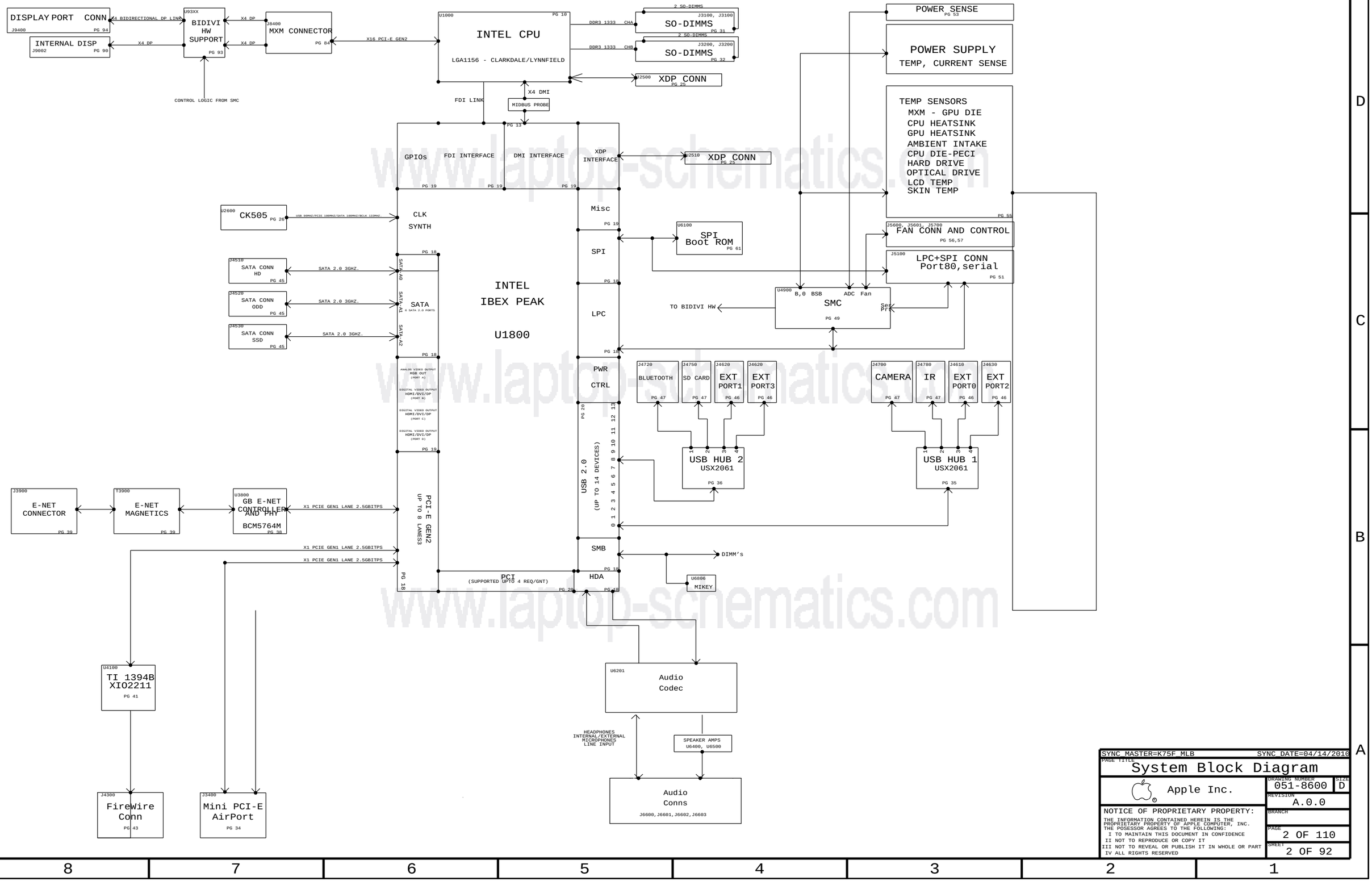
LAST_MODIFIED=Thu Apr 15 11:21:16 2010

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Thu Apr 15 11:21:16 2010

DRAWING TITLE: SCH,K75F,MLB_MEMSWAP

Apple Inc.

DRAWING NUMBER: 051-8600 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 110
SHEET: 1 OF 92



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

REVISION A.0.0

BRANCH

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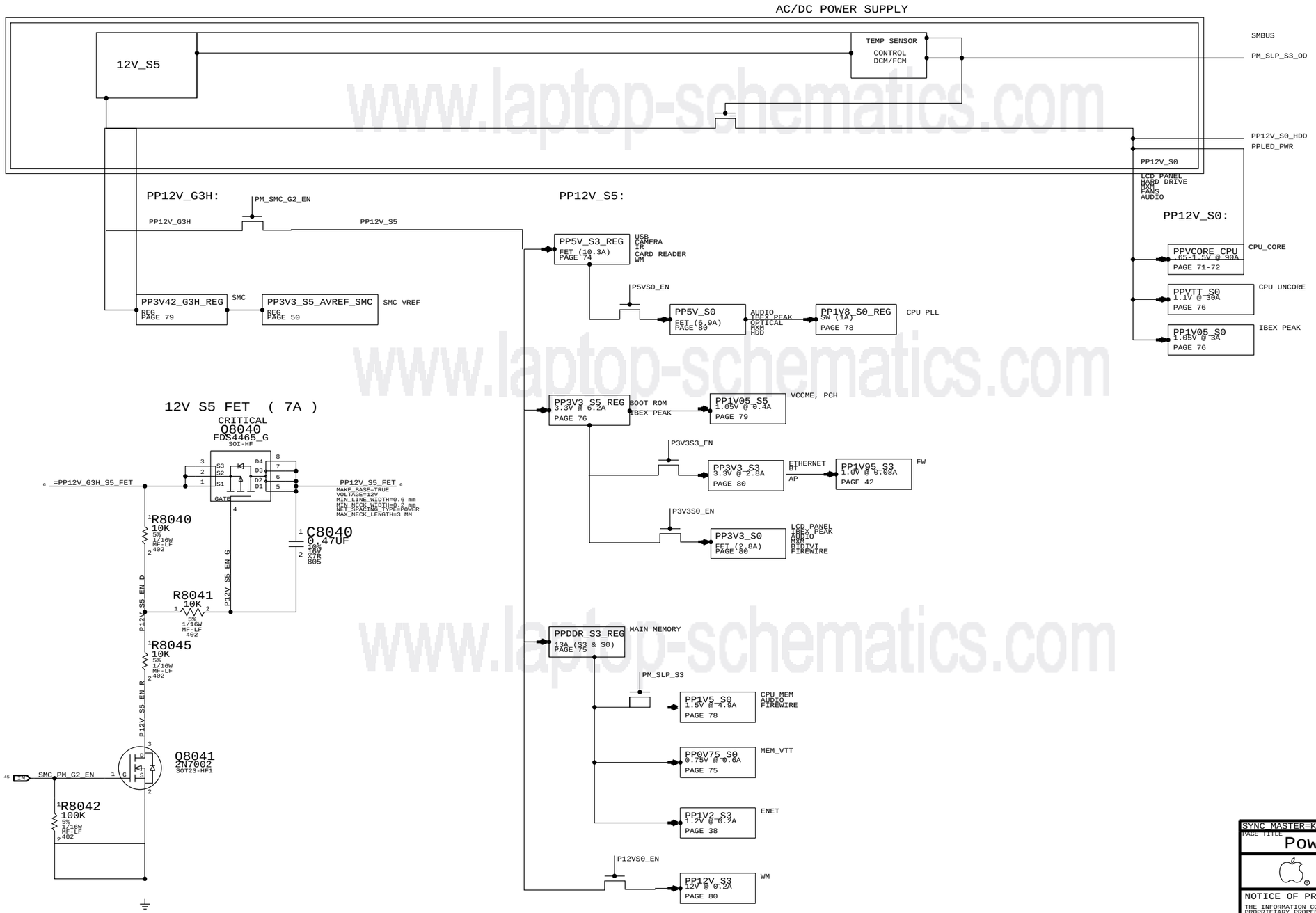
SHEET 2 OF 92



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Power Block Diagram

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-1609	PCBA,MLB,DEV,K75F	DEVELOPMENT,DEV_GROUP
639-1103	PCBA,MLB,K75F,3.20GHZ,CKD	K75F,3P20GHZ_CKD_CPU,BASIC,CPUPOC_IMAX_100_120
639-1105	PCBA,MLB,K75F,3.60GHZ,CKD	K75F,3P60GHZ_CKD_CPU,BASIC,CPUPOC_IMAX_100_120
639-1104	PCBA,MLB,K75F,2.66GHZ,LFD	K75F,2P66GHZ_LFD_CPU,BASIC,CPUPOC_IMAX_100_120
639-1106	PCBA,MLB,K75F,2.93GHZ,LFD	K75F,2P93GHZ_LFD_CPU,BASIC,CPUPOC_IMAX_100_120

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,XDP,BETTER,MXM,XDP_CPU_BPM,INT_VREF,PCH_VRM,BUF_CLK,PRODUCTION
DEV_GROUP	XDP_CONN,LPCPLUS,MOJOMUX,CPU_TDIODE

CPU SOCKET & ILM SUB-BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0063	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-0942	1	ASSY,PURCHASED,ILM,MOLEX,K75	ILM	CRITICAL	MOLEX_SOCKET
511S0069	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	FOXCONN_SOCKET
604-0988	1	ASSY,PURCHASED,ILM,FOXCONN,K75	ILM	CRITICAL	FOXCONN_SOCKET

ALTERNATE SOCKET VENDORS MUST USE MATCHING ILM

BOM NUMBER	BOM NAME	BOM OPTIONS
607-6876	SUB ASSY,CPU SOCKET,K75F,MOLEX	MOLEX_SOCKET
607-6877	SUB ASSY,CPU SOCKET,K75F,FOXCONN	FOXCONN_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
607-6876	1	MOLEX CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
607-6877	607-6876		SKT_ILM	FOXCONN ALTERNATIVE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S3828	1	IC,IBEX PEAK B3 PRQ,DESKTOP,FCBGA,P425	U1800	CRITICAL	
	359S0157	1	IC,SLG2AP108,CLK GEN,CK505,QFN3	U2600	CRITICAL	BUF_CLK
	341T0230	1	IC,EFI BOOTROM,K74/K75	U6100	CRITICAL	
	338S0765	1	IC,XIO2211ZAY,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	343S0485	1	IC,BCM5764M,68PIN QFN	U3700	CRITICAL	
RAW: 335S0663	341T0269	1	ENET 1MBIT FLASH,CII,K74/K75F	U3701	CRITICAL	
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3911	1	CKD,SLBUD,PRQ,3.20,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P20GHZ_CKD_CPU
337S3910	1	CKD,SLBTM,PRQ,3.60,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P60GHZ_CKD_CPU
337S3810	1	LFD,SLBLC,PRQ,2.66,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P66GHZ_LFD_CPU
337S3861	1	LFD,SLBJG,PRQ,2.93,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P93GHZ_LFD_CPU

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293		C7460,C7461,C7462,C7463	
518S0811	518S0685		J9002	

K75F PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-8600	1	SCH,K75F,MLB_MEMSWAP	SCH1		K75F
	820-2901	1	PCBF,K75F,MLB_MEMSWAP	MLB1		K75F
(338S0489 - BLNK)	341T0273	1	IC,SMC,K75F	U4900	CRITICAL	K75F

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

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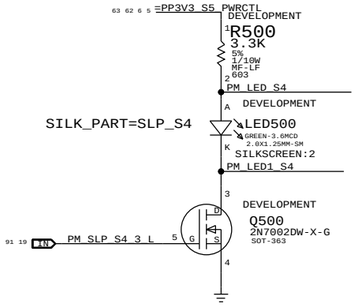
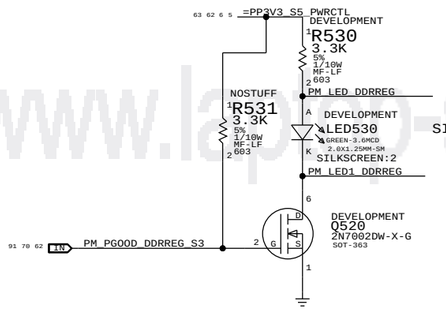
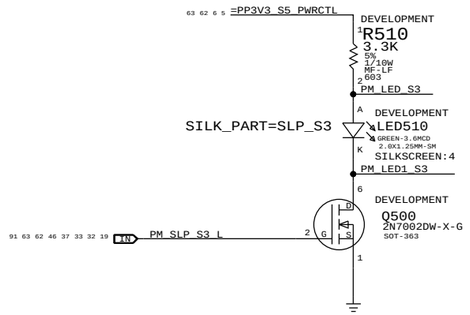
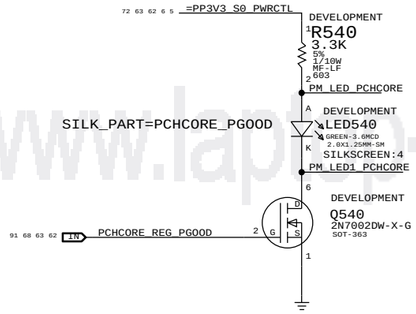
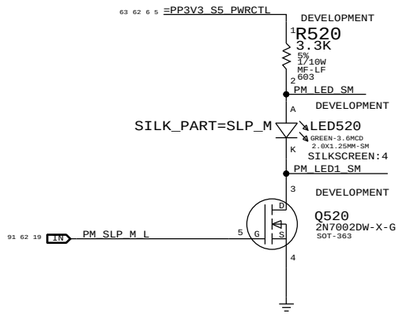
CAN DELETE THESE FOR PROTO1 AND BEYOND

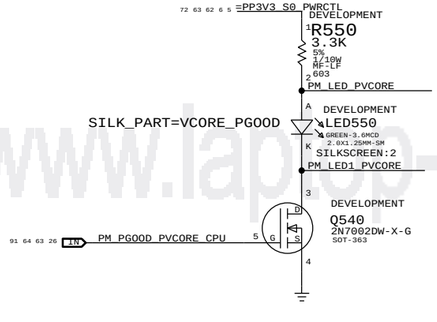












State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: PROTO 0 DEBUG LEDS

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

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EMC: C600,C626,C627,C628,C629,C630,C631

PLACE AT J600.

518-0352
CRITICAL
J600
76833-0100
M-RT-TH

=SMB_ACDC_SCL
=PP5V_S0_SATA
PP12V_G3H
LCD_PWM
=SMB_ACDC_SDA
PP12V_S0
LCD_BKL_ON

C623 10UF 20% 16V X5R 805
C631 0.001UF 10% 50V X7R 402
C627 0.001UF 10% 50V X7R 402
C626 0.001UF 10% 50V X7R 402
C630 0.001UF 10% 50V X7R 402
C624 10UF 10% 16V X5R-CERM 1210

PM_ACDC_PS_ON
PM_SLPS3_BUF2_L
Q610 2N7002 2SOT23-HF1
C600 0.001UF 10% 50V X7R 402

PP3V3_S3
R600 1K 5% 1/16W MF-LF 402
ITS_ALIVE
DEVELOPMENT
LED605 GREEN-3.6MCD 2.0X1.25MM-SM

PP3V3_S5_REG
R601 1K 5% 1/16W MF-LF 402
ITS_PLUGGED_IN
LED601 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:1

PP3V3_S3
R602 1K 5% 1/16W MF-LF 402
CORE_VOLTAGES_ON_R
LED602 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:2
CORE_VOLTAGES_ON
ALL_SYS_PWRGD_R
Q602 2N7002DW-X-G SOT-363

PP3V3_S0
R604 1K 5% 1/16W MF-LF 402
GPU_PRESENT_R
MXM LED604 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:3
GPU_PRESENT_DRAIN
MXM_GOOD
Q602 2N7002DW-X-G SOT-363

PP3V3_S0
R603 1K 5% 1/16W MF-LF 402
LCD_SHOULD_ON_R
LED603 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:4
VIDEO_ON_L

"S0" RAILS

ONLY ON IN RUN

PPVTT_S0_DDR
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVTT_S0_DDR_FET 32
→ =PP0V75_S0_MEM_VTT_B 31
→ =PP0V75_S0_MEM_VTT_A 30

PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVCORE_S0_CPU_REG 64 65 66
→ =PPVCORE_S0_CPU 13 16

PPVTT_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PPVTT_S0_CPU 11 13 16 46 64

PPVTT_S0
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVTT_S0_CPU_REG 49 67
→ =PPVTT_S0_PCH_VCC_DMI 22 24
→ =PPVTT_S0_XDP 25
→ =PPVTT_S0_PCH_VCCP_CPU 22 24

PP1V5_CPU_MEM
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP1V5_CPU_MEM 13 16 29

PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V5_S0_FET 49 72
→ =PP1V5_S0_AUD_DIG 55
→ =PP1V5_FWRS0_FWXIO 39
→ =PP1V5_S0_CK505 26

PP1V8_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP1V8_S0_CPU_PLL 13 16 63

PP1V8_S0
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V8_S0_REG 49 70
→ =PP3V3R1V8_S0_PCH_VCCPNAND 22 24
→ =PP1V8R1V5_S0_PCH_VCCVRM 24

PPVAXG_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PPVAXG_S0_CPU 13 17

PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_S0_FET 72
→ =PP3V3_S0_PCH 18 21 24 68
→ =PP3V3_S0_FAN 52 53
→ =PP3V3_S0_PCH_VCCADAC 17
→ =PPSPD_S0_MEM_A 30 46
→ =PPSPD_S0_MEM_B 31
→ =PP3V3_S0_VRD 64
→ =PP3V3_S0_AUDIO 55 57 58 59 60 61
→ =PP3V3R1V5_S0_PCH_VCCSUSHDA 22 24
→ =PP3V3_S0_SMBUS 48
→ =PP3V3_S0_SMC_LS 46 51
→ =PP3V3_S0_SMBUS_SMC_0_S0 48
→ =PP3V3_S0_SMBUS_SMC_B_S0 48
→ =PP3V3_S0_SMBUS_SMC_MGMT 48
→ =PP3V3_S0_DPCONN 80
→ =PP3V3_S0_TSENS 51
→ =PP3V3_S0_MXM 63 73 74
→ =PP3V3_S0_XDP 25
→ =PP3V3_S0_ODD 42
→ =PP3V3_S0_SATALED 18 42
→ =PP3V3_S0_SMC 46 49 50
→ =PP3V3_S0_PWRCTL 5 62 63 72
→ =PP3V3_S0_PCH_VCC3_3_CORE 22 24
→ =PP3V3_S0_VIDEO 77
→ =PP3V3_FW_FWPHY 39 40 41
→ =PP3V3_FWRS0_FWXIO 39
→ =PP3V3_S0_DP 77 78 79 81
→ =PP3V3_S0_PCH_VCC3_3_PCI 22 24
→ =PP3V3_S0_CK505 26
→ =PP3V3_S0_PCH_GPIO 20
→ =PP3V3_S0_PCH_STRAPS 15
→ =PP3V3_S0_PCH_VCC3_3_SATA 22 24
→ =PP3V3_S0_RSTBUF 27
→ =PP3V3_S0_ME 72
→ =PP3V3_S0_ENET 36
→ =PP3V3_S0_PCH_PM 27
→ =PP3V3_S0_SMBUS_SMC_BSA 48

PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP5V_S0_FET 72
→ =PP5V_S0_AUDIO 55 61
→ =PP5V_S0_SATA 6 42
→ =PP5V_S0_MXM 73
→ =PP5V_S0_VRD 64
→ =PP5V_S0_ISENSE 49
→ =PP5V_S0_P1V8_VREG 70
→ =PP5V_S0_PCH 24
→ =PP5V_S0_CPU_VTT_VREG 67
→ =PP5V_S0_LPCPLUS 47
→ =PP5V_S0_PCH_CORE_VREG 68

PP1V05_S0
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V05_S0_REG 68
→ =PP1V05_S0_PCH_VCCADPLL 17
→ =PP1V05_S0_PCH_VCCIO_DMI 22 24
→ =PP1V05_S0_PCH 24
→ =PP1V05_S0_SM_FET 72
→ =PP1V05_S0_PCH_VCCIO_SATA 18 22 24
→ =PP1V05_S0_PCH_VCCIO_PCIE 18 19 22 24
→ =PP1V05_S0_PCH_VCC_CORE 22 24
→ =PP1V05_S0_PCH_VCCIO_USB 22 24
→ =PP1V05_S0_CK505 26

PP1V05_SM_PCH_LAN
MAKE_BASE=TRUE
VOLTAGE=1.05V
THIS NET IS NOT CONNECTED TO ANY VOLTAGE RAIL. INSTEAD ON PAGE 24 IT IS CONNECTED TO GND THROUGH A RESISTOR
→ =PP1V05_SM_PCH_VCC_LAN 22 24

PP0V75_S0
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVTT_S0_DDR_LDO 70
→ =PP0V75_S0_MEM_VTT_S0FET 32

PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP12V_S0_FAN 52 53
→ =PP12V_S0_AUDIO_SPKRAMP 60
→ =PP12V_S0_VRD 64
→ =PPV_S0_MXM_PWR 50
→ =PP12V_S0_LCD 77
→ =PP12V_S0_PCH_CORE_VREG 68
→ =PP12V_S0_CPU_VTT_VREG 67
→ =PP12V_S0_PWRCTL 63

"S3" RAILS

ON IN RUN AND SLEEP

PP1V5_S3
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V5_S3_REG 49 50 70
→ =PP1V5_S3_MEMRESET 32
→ =PPDDR_S3_S0FET 72
→ =PP1V5_S3_MEM_A 28 29 30
→ =PP1V5_S3_MEM_B 28 29 31

PP12V_S3
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP12V_S3_FET 72
→ =PP12V_S3_WM 44

PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_S3_FET 72
→ =PP3V3_S3_VREFMRGN 28
→ =PP3V3_S3_BT 44
→ =PP3V3_S3_PCH_STRAPS 15
→ =PP3V3_S3_SDCARD 44
→ =PP3V3_S3_SMBUS_SMC_A_S3 48
→ =PP3V3_S3_MINI 33
→ =PP3V3_S3_PWRCTL 63 72
→ =PP3V3_S3_WM 44
→ =PP3V3_S3_SMBUS 48
→ =PP3V3_S3_MEMRESET 32
→ =PP3V3_S3_BRCRYPT 44
→ =PP3V3_S3_ENET 37
→ =PP3V3_S3_USB_HUB 34 35
→ =PP3V3_S3_USB_RESET 34

PP5V_S3
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP5V_S3_REG 69 92
→ =PP5V_S3_USB 43
→ =PP5V_S3_S0FET 72
→ =PP5V_S3_CAMERA 44
→ =PP5V_S3_IR 44
→ =PP5V_S3_VREFMRGN 28
→ =PP5V_S3_PWRCTL 62
→ =PP5V_S3_MEMRESET 32
→ =PP5V_S3_DDR_VREG 70
→ =PP5V_S3_BRAY 44

PP3V3_S0M
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_SM_FET 72
→ =PP3V3_SM_PCH_VCC_ME 22 24
→ =PP3V3_SM_PWRCTL 63 72

PP1V05_SM
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V05_SM_FET 72
→ =PP1V05_SM_PCH_VCC_ME 22 24
→ =PP1V05_SM_ME 63

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

PP1V05_S5
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V05_S5_REG 71
→ =PP1V05_S5_SM_FET 72

PP3V3_S5
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_S5_REG 6 69
→ =PP3V3_S5_PCH 18 19 24
→ =PP3V3_S5_PCH_GPIO 20
→ =PP3V3_S5_ROM 47 54
→ =PP3V3_S5_PCH_VCCSUS3_3_USB 22 24
→ =PP3V3_S5_PWRCTL 5 62 63
→ =PP3V3_S5_S3FET 72
→ =PP3V3_S5_S0FET 72
→ =PP3V3_S5_P1V05S5_VREG 71
→ =PP3V3_S5_SM_FET 72
→ =PP3V3_S5_PCH_STRAPS 15
→ =PP3V3_S5_CPURESET 11
→ =PP3V3_S5_XDP 25
→ =PP3V3_S5_MEMRESET 32
→ =PP3V3_S5_LPCPLUS 47

PP5V_S5
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP5V_S5_LDO 69
→ =PP5V_S5_PCH 24

PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP12V_S5_FET 3
→ =PP12V_S5_DDR_VREG 70
→ =PP12V_S5_P3V3S5_VREG 69
→ =PP12V_S5_P5VS3_VREG 69
→ =PP12V_S5_S3_FET 72
→ =PP12V_S5_PWRCTL 63 72
→ =PP12V_S5_FW 41

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

PP3V42_G3H
MAKE_BASE=TRUE
VOLTAGE=3.42V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V42_G3H_REG 71
→ =PP3V3_S5_RTC_D 27
→ =PP3V3_G3H_SMC 45 46
→ =PP3V3_G3H_SMCUSBMUX 43
→ =PP3V42_G3H_AVREF 46
→ =PP3V3_G3H_LPCPLUS 47

PP12V_G3H
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP12V_G3H_S5_FET 3

GND RAILS

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: Power Conn / Alias

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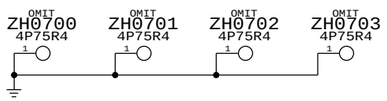
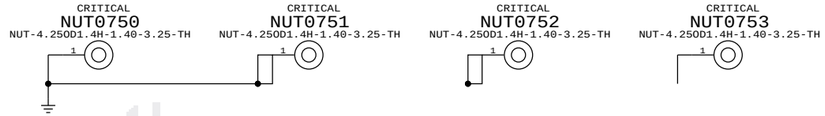
CPU Heatsink

4mm Plated Holes (998-0850)



DIMM CONNECTOR NUTS

Nuts (805-9582)



PCH HEATSINK

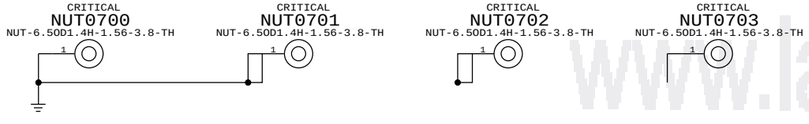
EMC Springs (870-1125) Removed 2009-10-05

Rear Cover

Standoffs (860-1255)

Backer Plate

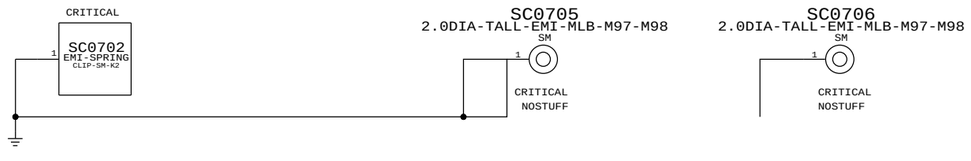
Nuts (835-0269)



For EMC

EMC Spring (870-1577); Near DIMMs

EMC POGO Pins (870-1698); Near DIMMs



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

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UNUSED CPU SIGNALS

10 TP_CPU_RSVD<41..29> — NC_CPU_RSVD<41..29> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_CPU_RSVD<26..1> — NC_CPU_RSVD<26..1> MAKE_BASE=TRUE NO_TEST=TRUE
13 TP_CPU_FC_AE38 — NC_CPU_FC_AE38 MAKE_BASE=TRUE NO_TEST=TRUE
13 TP_CPU_FC_AG40 — NC_CPU_FC_AG40 MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

20 TP_PCI_AD<31..0> — NC_PCI_AD<31..0> MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_PCI_C_BE_L<3..0> — NC_PCI_C_BE_L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE

20 TP_PCI_PAR — NC_PCI_PAR MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_PCI_RESET_L — NC_PCI_RESET_L MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCIE_CLK100M_XDPP — NC_PCIE_CLK100M_XDPP MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCIE_CLK100M_XDPN — NC_PCIE_CLK100M_XDPN MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_DMI_CLK100M_LAP — NC_DMI_CLK100M_LAP MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_DMI_CLK100M_LAN — NC_DMI_CLK100M_LAN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_LPC_DREQ1_L — NC_LPC_DREQ1_L MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_LPC_DREQ0_L — NC_LPC_DREQ0_L MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED NAND ALIASES

20 TP_NV_CE_L<3..0> — NC_NV_CE_L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_NV_DQS<1..0> — NC_NV_DQS<1..0> MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_NV_DQ<15..0> — NC_NV_DQ<15..0> MAKE_BASE=TRUE NO_TEST=TRUE

20 TP_NV_RB_L — NC_NV_RB_L MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_NV_WR_RE_L<1..0> — NC_NV_WR_RE_L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_NV_WE_CK_L<1..0> — NC_NV_WE_CK_L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

25 TP_JTAG_XDP_TRST_L — NC_JTAG_XDP_TRST_L MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM0 — NC_PCH_PWM0 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM1 — NC_PCH_PWM1 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM2 — NC_PCH_PWM2 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM3 — NC_PCH_PWM3 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_SST — NC_PCH_SST MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

12 TP_MEM_A_CS_L<7..4> — NC_MEM_A_CS_L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_A_DQ_CB<7..0> — NC_MEM_A_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
83 12 TP_MEM_A_DQS_N<8> — NC_MEM_A_DQS_N<8> MAKE_BASE=TRUE NO_TEST=TRUE
83 12 TP_MEM_A_DQS_P<8> — NC_MEM_A_DQS_P<8> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_B_CS_L<7..4> — NC_MEM_B_CS_L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_B_DQ_CB<7..0> — NC_MEM_B_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
83 12 TP_MEM_B_DQS_N<8> — NC_MEM_B_DQS_N<8> MAKE_BASE=TRUE NO_TEST=TRUE
83 12 TP_MEM_B_DQS_P<8> — NC_MEM_B_DQS_P<8> MAKE_BASE=TRUE NO_TEST=TRUE

TP_PCI_T28_D2R_N<3..0> — NC_PCI_T28_D2R_N<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCI_T28_D2R_P<3..0> — NC_PCI_T28_D2R_P<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCI_T28_R2D_C_N<3..0> — NC_PCI_T28_R2D_C_N<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCI_T28_R2D_C_P<3..0> — NC_PCI_T28_R2D_C_P<3..0> MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_HDA_SDIN1 — NC_HDA_SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_HDA_SDIN2 — NC_HDA_SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_HDA_SDIN3 — NC_HDA_SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCIE_CLK100M_PE5P — NC_PCIE_CLK100M_PE5P MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_CLK100M_PE5N — NC_PCIE_CLK100M_PE5N MAKE_BASE=TRUE NO_TEST=TRUE

20 TP_NV_RCOMP — NC_NV_RCOMP MAKE_BASE=TRUE NO_TEST=TRUE

18 PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARD_P MAKE_BASE=TRUE NO_TEST=TRUE
18 PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARD_N MAKE_BASE=TRUE NO_TEST=TRUE

20 TP_USB_7N — NC_USB_7N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_7P — NC_USB_7P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_6N — NC_USB_6N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_6P — NC_USB_6P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_1N — NC_USB_1N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_1P — NC_USB_1P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_3N — NC_USB_3N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_3P — NC_USB_3P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_5N — NC_USB_5N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_5P — NC_USB_5P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_9N — NC_USB_9N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_9P — NC_USB_9P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_10N — NC_USB_10N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_10P — NC_USB_10P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_11N — NC_USB_11N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_11P — NC_USB_11P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_12N — NC_USB_12N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_12P — NC_USB_12P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_13N — NC_USB_13N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_13P — NC_USB_13P MAKE_BASE=TRUE NO_TEST=TRUE

18 PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2R_P MAKE_BASE=TRUE NO_TEST=TRUE
18 PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2R_N MAKE_BASE=TRUE NO_TEST=TRUE
18 PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_C_P MAKE_BASE=TRUE NO_TEST=TRUE
18 PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_C_N MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_TVCLKINN — NC_SDVO_TVCLKINN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_TVCLKINP — NC_SDVO_TVCLKINP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_STALLN — NC_SDVO_STALLN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_STALLP — NC_SDVO_STALLP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_INTN — NC_SDVO_INTN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_INTP — NC_SDVO_INTP MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

18 TP_SATA_D_D2RN — NC_SATA_D_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_D_D2RP — NC_SATA_D_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_D_R2D_CN — NC_SATA_D_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_D_R2D_CP — NC_SATA_D_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_D2RN — NC_SATA_E_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_D2RP — NC_SATA_E_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_R2D_CN — NC_SATA_E_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_R2D_CP — NC_SATA_E_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_D2RN — NC_SATA_F_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_D2RP — NC_SATA_F_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_R2D_CN — NC_SATA_F_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_R2D_CP — NC_SATA_F_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

19 TP_CRT_IG_DDC_CLK — NC_CRT_IG_DDC_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_DDC_DATA — NC_CRT_IG_DDC_DATA MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_RED — NC_CRT_IG_RED MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_GREEN — NC_CRT_IG_GREEN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_BLUE — NC_CRT_IG_BLUE MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_HSYNC — NC_CRT_IG_HSYNC MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_VSYNC — NC_CRT_IG_VSYNC MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_B_MLN<3..0> — NC_DP_IG_B_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_MLP<3..0> — NC_DP_IG_B_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_AUX_N — NC_DP_IG_B_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_AUX_P — NC_DP_IG_B_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_HPD — NC_DP_IG_B_HPD MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_DDC_CLK — NC_DP_IG_B_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_DDC_DATA — NC_DP_IG_B_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_MLN<3..0> — NC_DP_IG_C_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_MLP<3..0> — NC_DP_IG_C_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_AUX_N — NC_DP_IG_C_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_AUX_P — NC_DP_IG_C_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_HPD — NC_DP_IG_C_HPD MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_CTRL_CLK — NC_DP_IG_C_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_CTRL_DATA — NC_DP_IG_C_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_MLN<3..0> — NC_DP_IG_D_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_MLP<3..0> — NC_DP_IG_D_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_AUXN — NC_DP_IG_D_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_AUXP — NC_DP_IG_D_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_HPD — NC_DP_IG_D_HPD MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_CTRL_CLK — NC_DP_IG_D_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_CTRL_DATA — NC_DP_IG_D_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

13 TP_GFX_VID<0..6> — NC_GFX_VID<0..6> MAKE_BASE=TRUE NO_TEST=TRUE
13 TP_GFX_VSENSE_N — NC_GFX_VSENSE_N MAKE_BASE=TRUE NO_TEST=TRUE
13 TP_GFX_VSENSE_P — NC_GFX_VSENSE_P MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
UNUSED SIGNAL ALIAS

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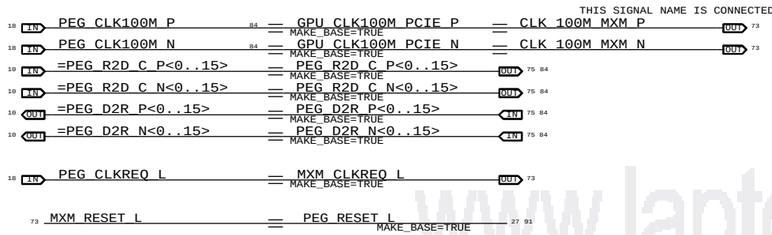
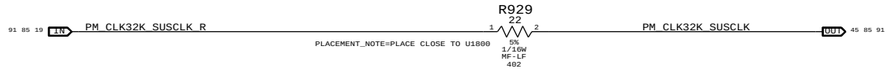
PEG Slot Support

THIS SIGNAL NAME IS CONNECTED TO MXM





SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: Signal Aliases

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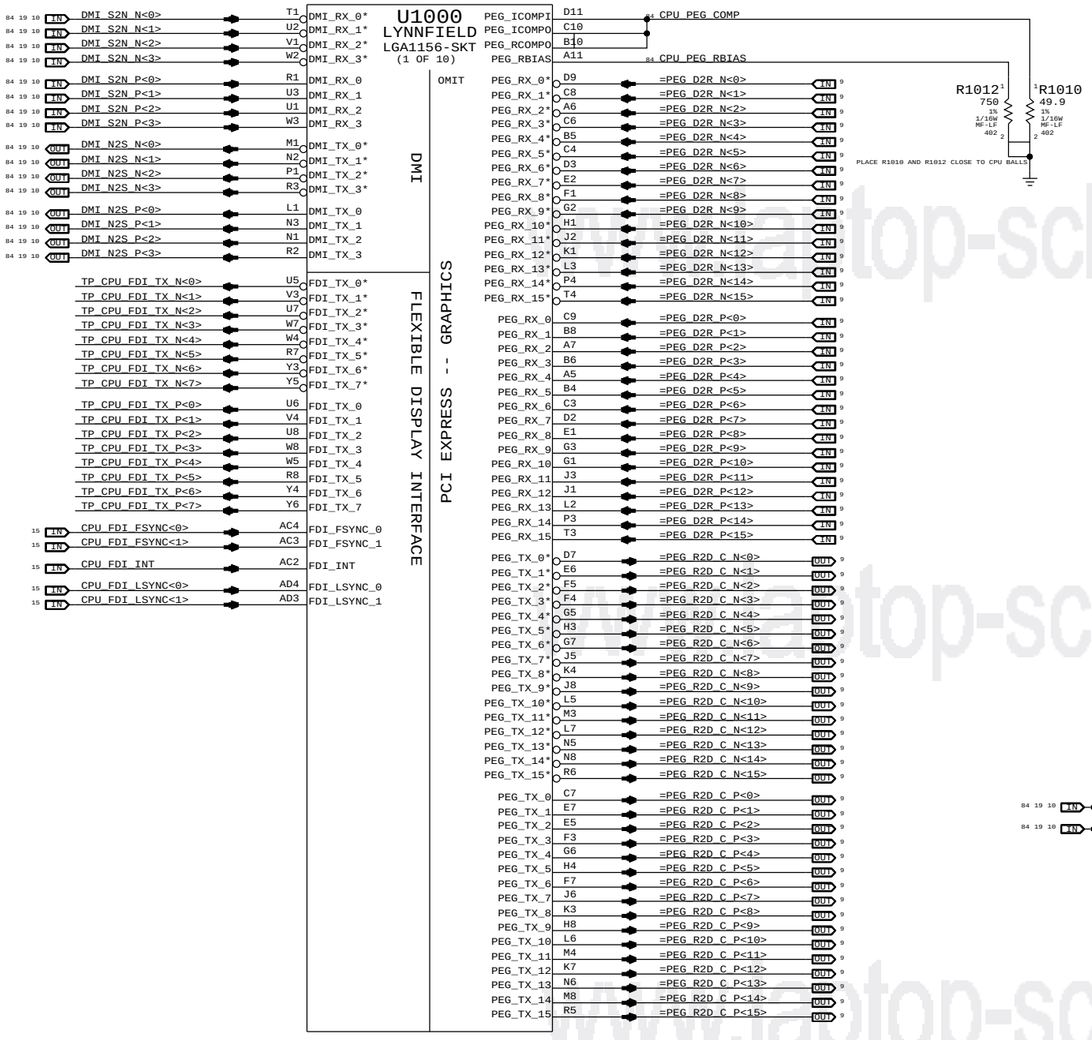

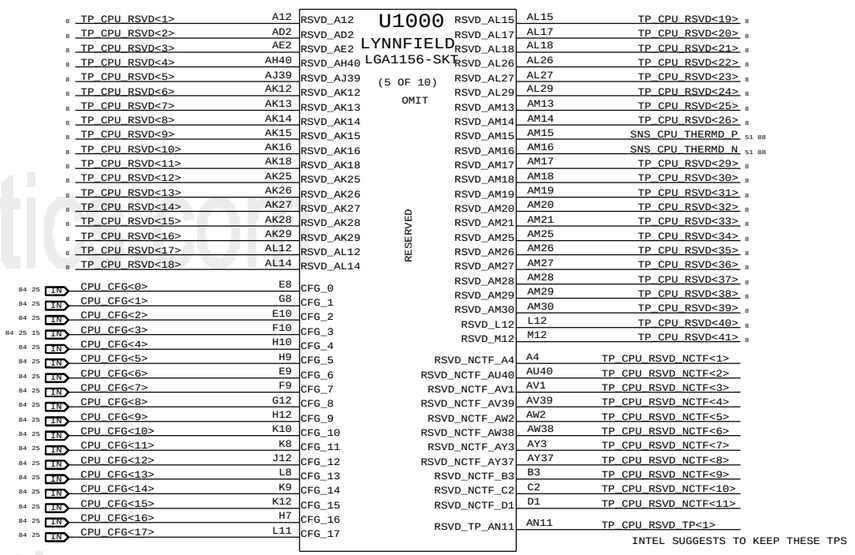

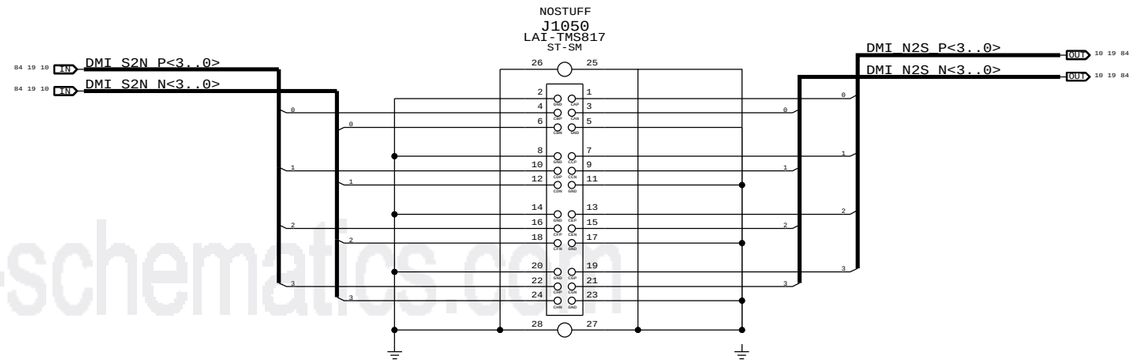

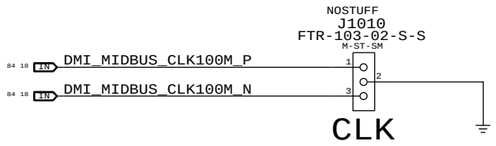

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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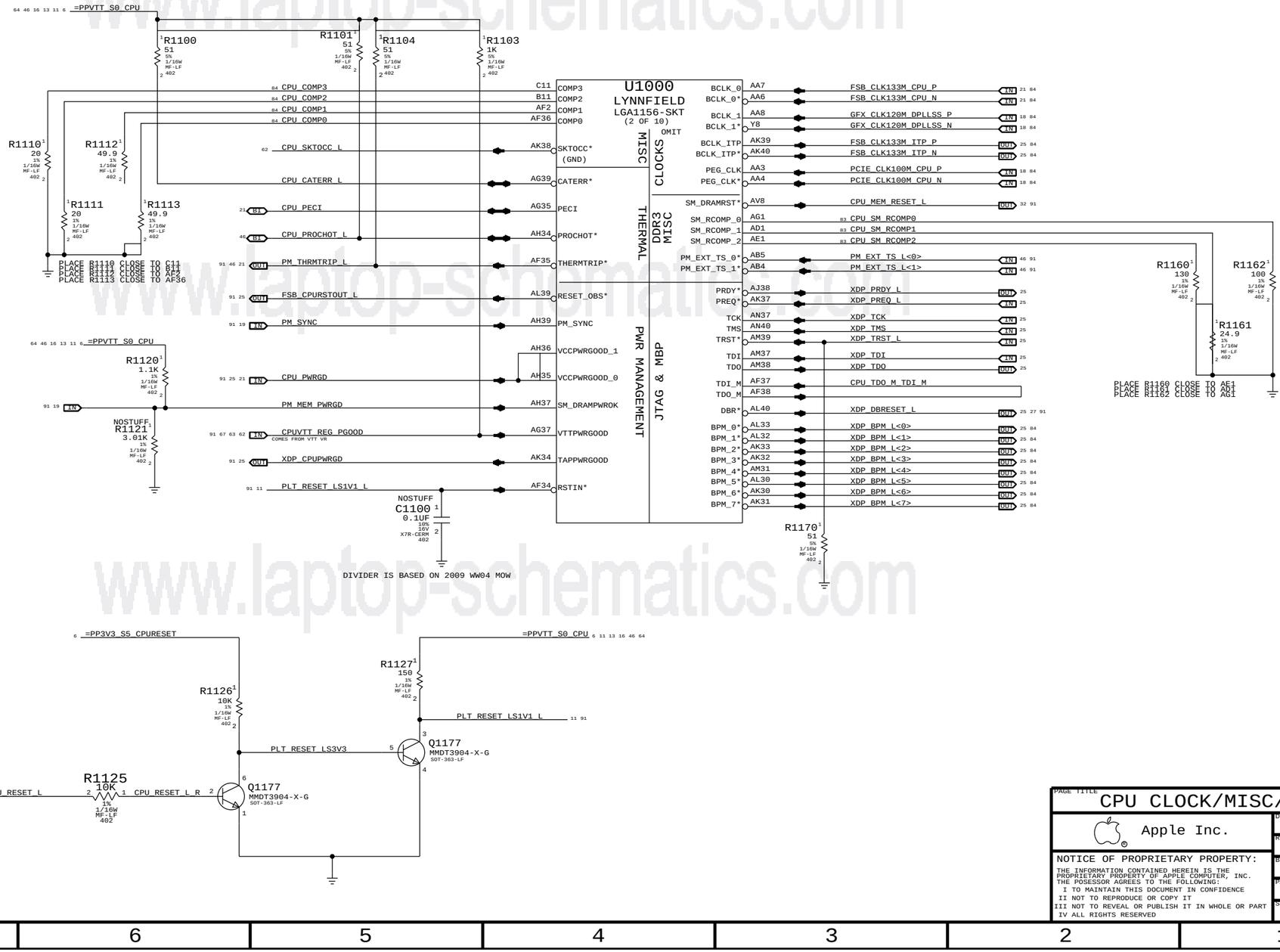

PAGE TITLE
CPU CLOCK/MISC/JTAG

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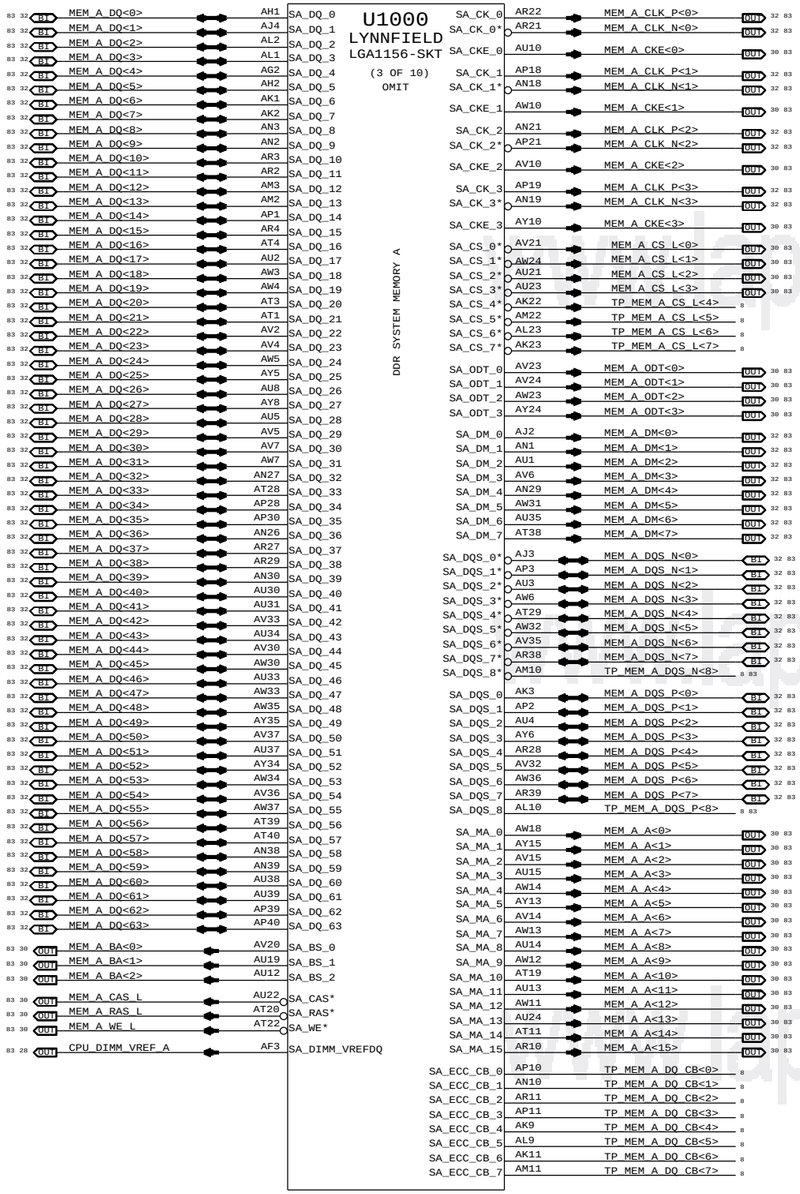

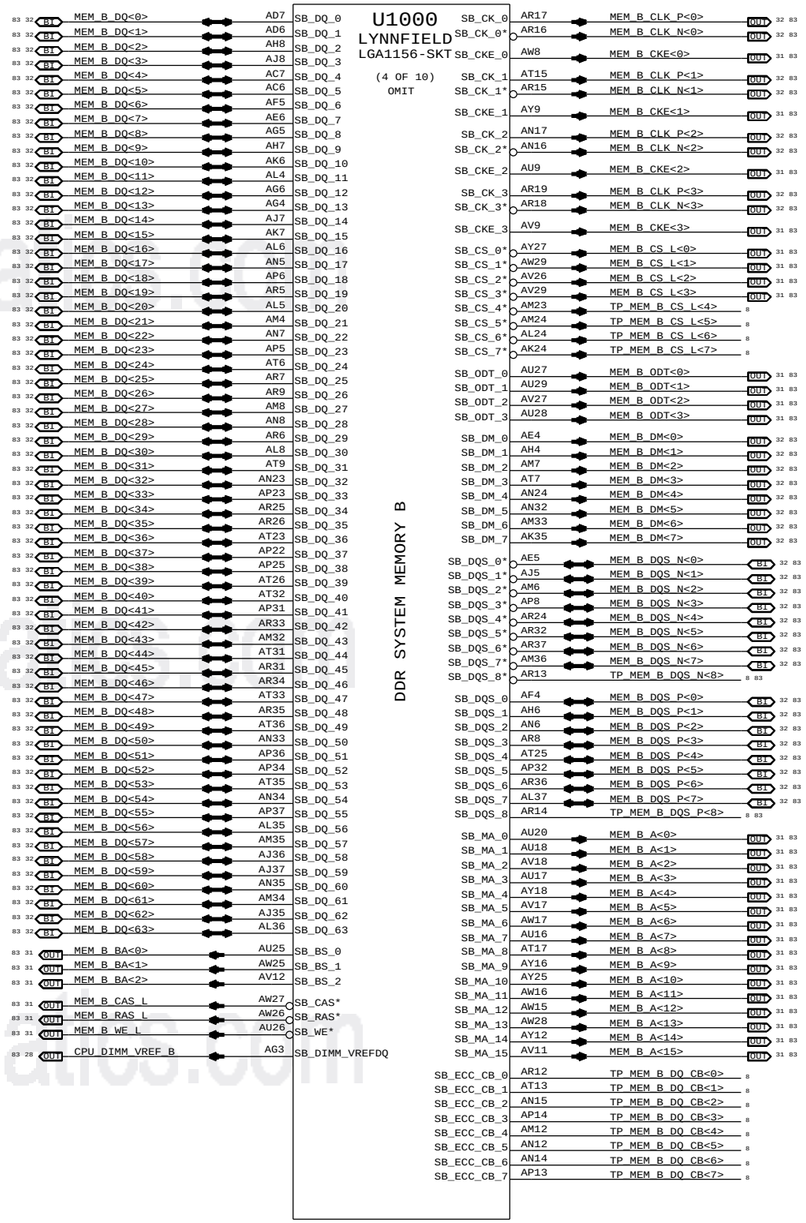

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PAGE TITLE
CPU DDR3 INTERFACES

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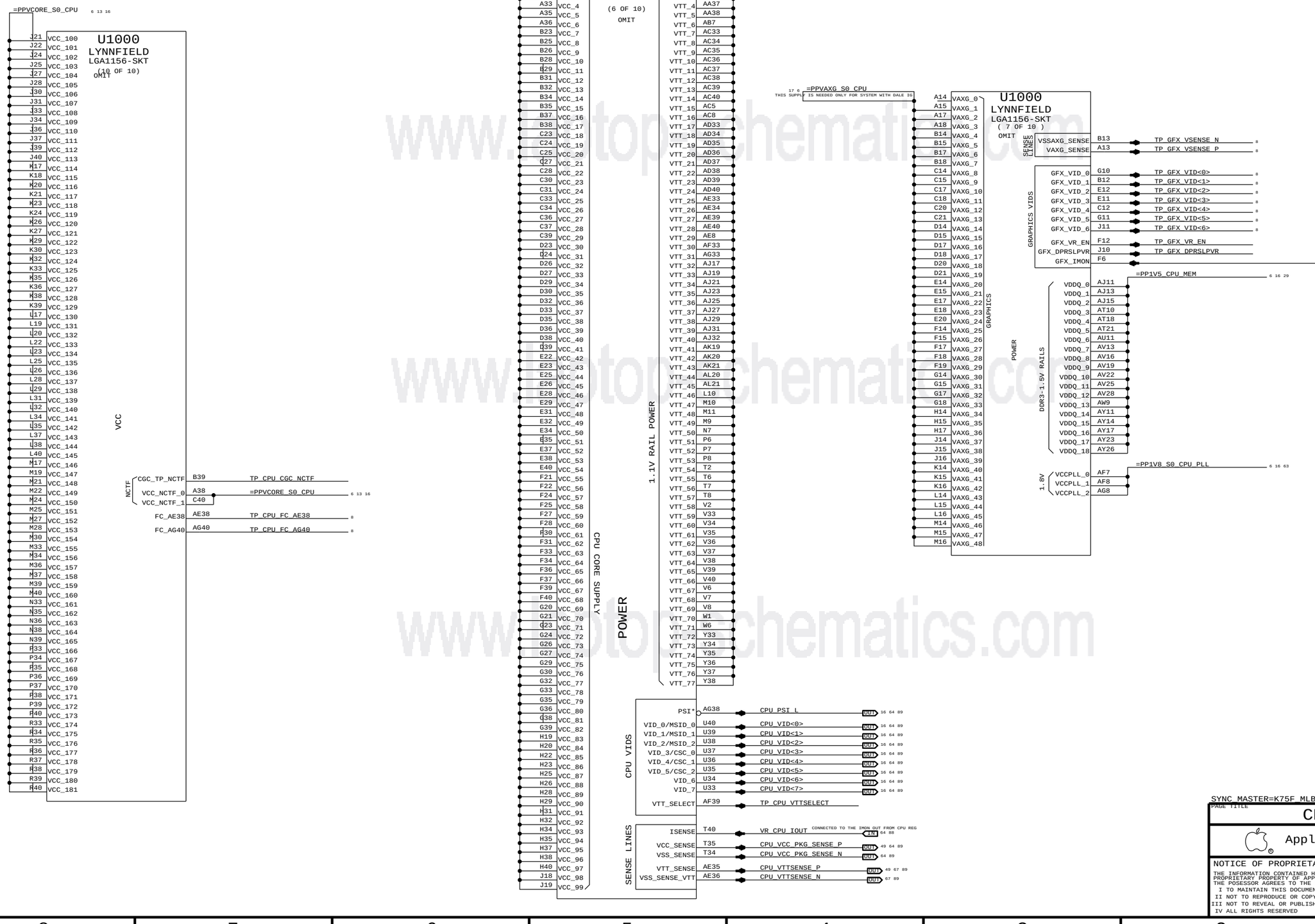

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
CPU POWER

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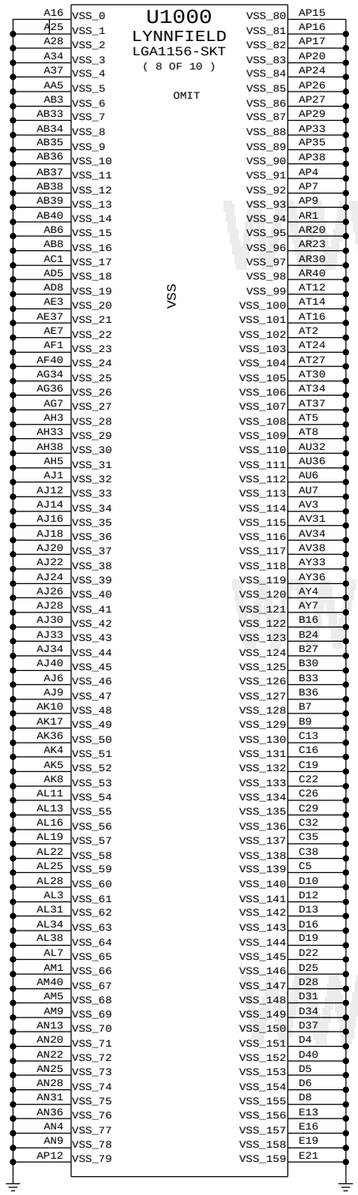

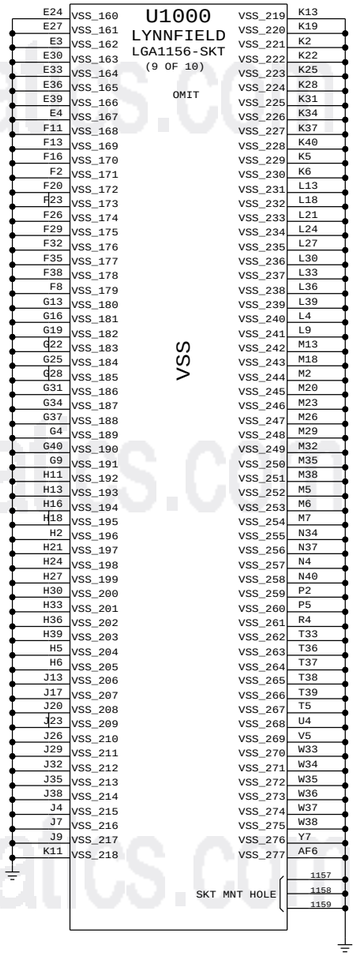

PAGE TITLE
CPU GROUNDS

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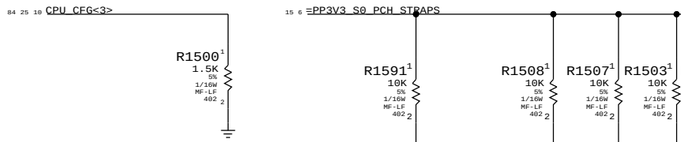

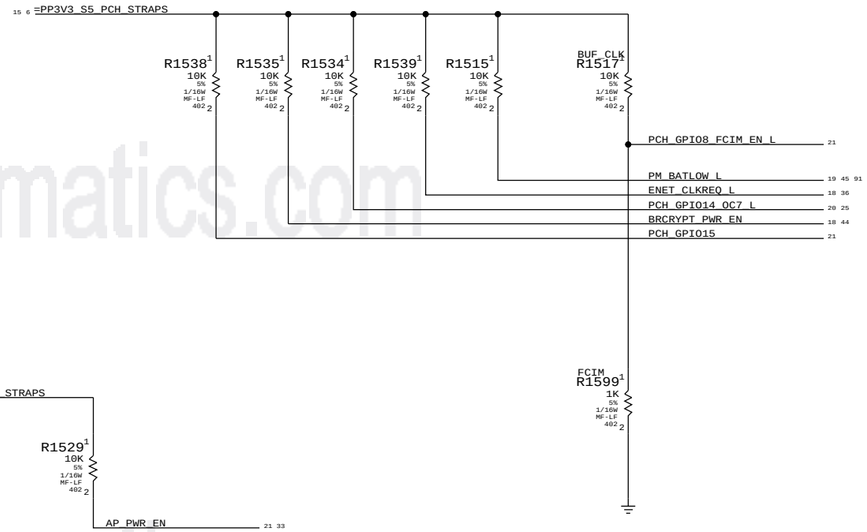

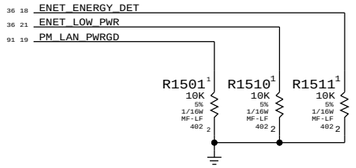

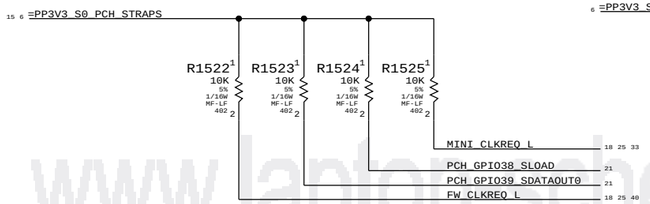

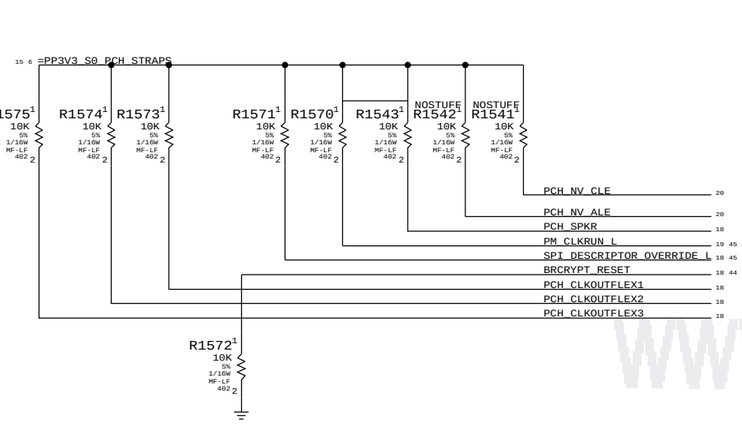

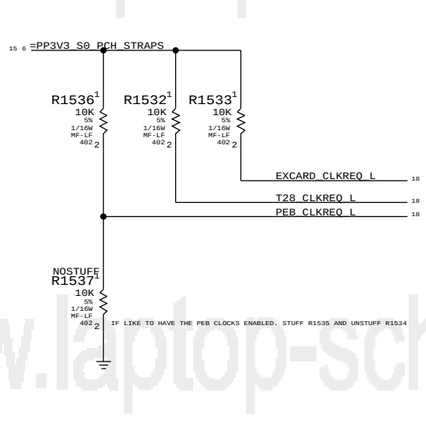

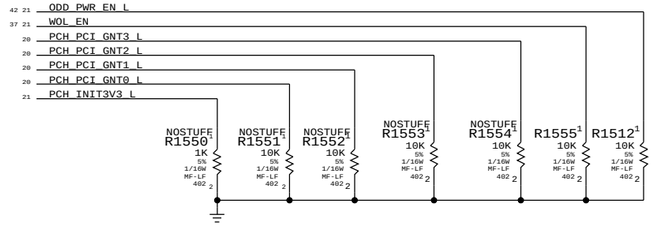

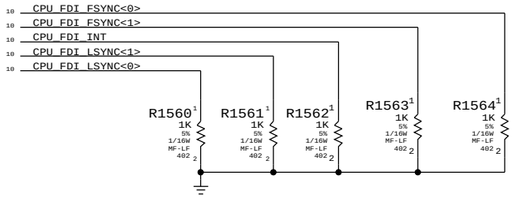

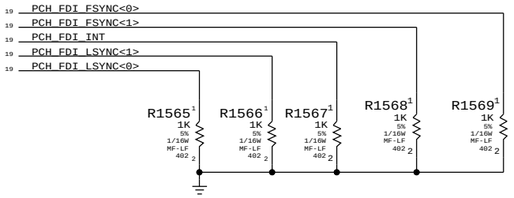

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STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

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CPU VCORE DECOUPLING

INTEL RECOMMENDATION 17X 22UF 0805

13 6 =PPVCORE_S0_CPU

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609
22UF 20% 6.3V CERM-X5R 805-3

C1610 C1611 C1612 C1613 C1614 C1615 C1616 NOSTUFF C1617 NOSTUFF C1618 NOSTUFF C1619
22UF 20% 6.3V CERM-X5R 805-3

BULK CAPS ON CPU VREG PAGE 74

VTT (CPU Uncore) DECOUPLING

8X 22UF 0805, 7X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805

64 46 16 13 11 6 =PPVTT_S0_CPU

PLACEMENT_NOTE (C1650-C1657):
Place under socket cavity on secondary side.

C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657
22UF 20% 6.3V CERM-X5R 805

PLACEMENT_NOTE (C1660-C1666):
Place at edge of socket.

C1660 C1661 C1662 C1663 C1664 C1665 C1666
10uF 20% 6.3V X5R 603

BULK CAPS ON CPU VREG PAGE 72

Memory (CPU VCCDDR) DECOUPLING

2x 22uF 0805, 5x 1uF 0402

29 13 6 =PP1V5_CPU_MEM

C1680 22uF 20% 6.3V CERM-X5R 805
C1681 22uF 20% 6.3V CERM-X5R 805
C1682 C1683 C1684 C1685 C1686
1UF 10% 10V X5R 402

PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402

63 13 6 =PP1V8_S0_CPU_PLL

C1690 22uF 20% 6.3V CERM-X5R 805
C1691 4.7UF 10% 6.3V X5R-CERM 603
C1692 2.2UF 10% 6.3V X5R 402
C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout

64 46 16 13 11 6 =PPVTT_S0_CPU

NO STUFF R1600 1K 5% 1/16W MF-LF 402
R1602 1K 5% 1/16W MF-LF 402
CPUPOC4U R1604 1K 5% 1/16W MF-LF 402
NO STUFF R1606 1K 5% 1/16W MF-LF 402
NO STUFF R1608 1K 5% 1/16W MF-LF 402

R1601 1K 5% 1/16W MF-LF 402
CPUPOC3U R1603 1K 5% 1/16W MF-LF 402
CPUPOC5U R1605 1K 5% 1/16W MF-LF 402
NO STUFF R1607 1K 5% 1/16W MF-LF 402

89 64 13 OUT CPU_VID<0>
89 64 13 OUT CPU_VID<1>
89 64 13 OUT CPU_VID<2>
89 64 13 OUT CPU_VID<3>
89 64 13 OUT CPU_VID<4>
89 64 13 OUT CPU_VID<5>
89 64 13 OUT CPU_VID<6>
89 64 13 OUT CPU_VID<7>
89 64 13 OUT CPU_PSI_L

R1610 1K 5% 1/16W MF-LF 402
NO STUFF R1612 1K 5% 1/16W MF-LF 402
CPUPOC4D R1614 1K 5% 1/16W MF-LF 402
R1616 1K 5% 1/16W MF-LF 402
NO STUFF R1618 1K 5% 1/16W MF-LF 402

NO STUFF R1611 1K 5% 1/16W MF-LF 402
CPUPOC3D R1613 1K 5% 1/16W MF-LF 402
CPUPOC5D R1615 1K 5% 1/16W MF-LF 402
R1617 1K 5% 1/16W MF-LF 402

VID[2:0] = FUNCTION MSI[2:0] DEFAULT (110)
VID[5:3] = IMON CONFIG DEFAULT (101)
VID[6] = Reserved (0)
VID[7] = VRD SELECT (0)
PSI# = Reserved (0)

MSI - MARKET SEGMENT IDENTIFICATION
PREVENTS THE PLATFORM BOOTING USING A HIGHER POWERED CPU

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_40	40A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_40_60	60A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_60_80	80A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_80_100	100A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_100_120	120A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_120_140	140A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_140_180	180A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly.
Instead call out appropriate BOM GROUP defined in tables above.

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CPU NON-GFX DECOUPLING

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13 6 =PPVAXG_S0_CPU

Grounding the Rail because Integrated Graphics wont be used

R1700
0
5%
1/16W
MF-LF
402

6 =PP3V3_S0_PCH_VCCADAC

69 mA

R1750
0
5%
1/16W
MF-LF
402

PP3V3_S0_PCH_VCCA_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

69 mA 22 89

6 =PP1V05_S0_PCH_VCCADPLL

150 MA

R1760
0
5%
1/16W
MF-LF
402

PP1V05_S0_PCH_VCCADPLLA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

75 MA 22 89

R1765
0
5%
1/16W
MF-LF
402

PP1V05_S0_PCH_VCCADPLLB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

75 MA 22 89

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
CPU/PCH GFX DECOUPLING

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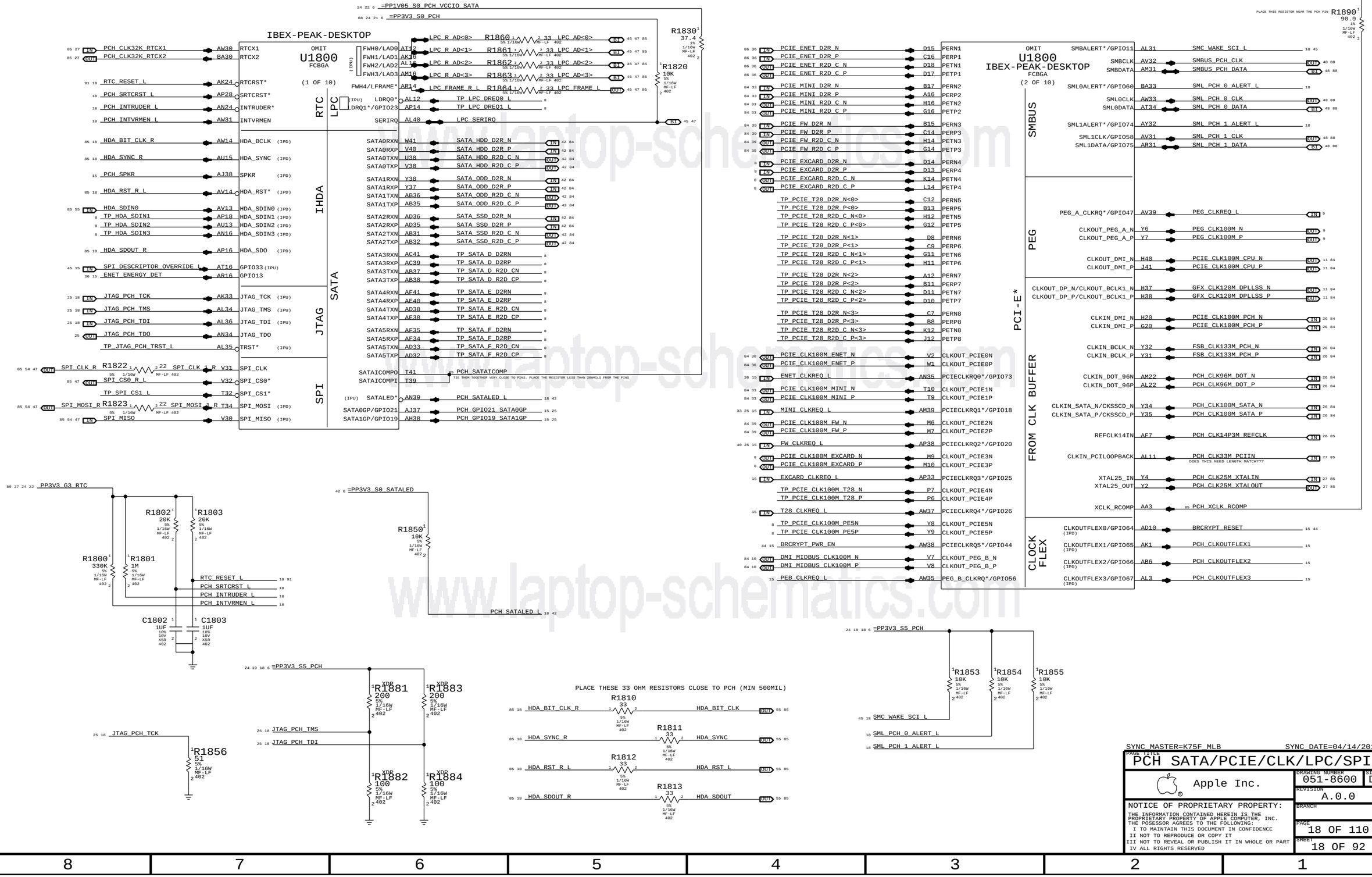

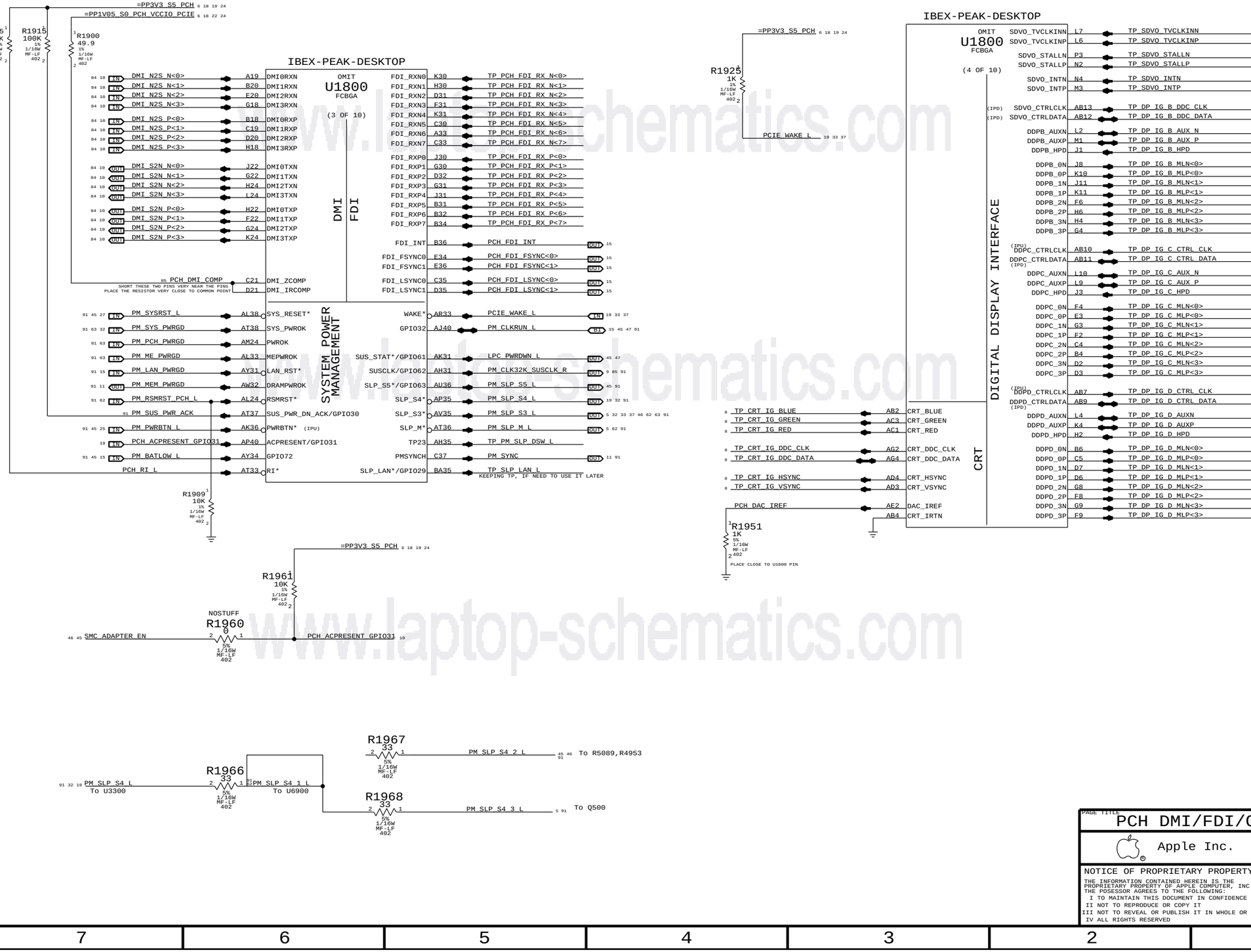

PAGE TITLE
PCH DMI/FDI/GRAPHICS

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IBEX-PEAK-DESKTOP

OMIT
U1800
FCBGA
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PCI

TP_PCI_AD<0>	AT9	AD0	
TP_PCI_AD<1>	AP11	AD1	
TP_PCI_AD<2>	AU6	AD2	
TP_PCI_AD<3>	AY10	AD3	
TP_PCI_AD<4>	AP9	AD4	
TP_PCI_AD<5>	AV8	AD5	
TP_PCI_AD<6>	AR9	AD6	
TP_PCI_AD<7>	AV7	AD7	
TP_PCI_AD<8>	AW9	AD8	
TP_PCI_AD<9>	AR3	AD9	
TP_PCI_AD<10>	AW7	AD10	
TP_PCI_AD<11>	AR8	AD11	
TP_PCI_AD<12>	AU3	AD12	
TP_PCI_AD<13>	AP2	AD13	
TP_PCI_AD<14>	AU1	AD14	
TP_PCI_AD<15>	AN3	AD15	
TP_PCI_AD<16>	AM2	AD16	
TP_PCI_AD<17>	AM11	AD17	
TP_PCI_AD<18>	AM4	AD18	
TP_PCI_AD<19>	AY8	AD19	
TP_PCI_AD<20>	AL10	AD20	
TP_PCI_AD<21>	AT5	AD21	
TP_PCI_AD<22>	AL2	AD22	
TP_PCI_AD<23>	AT2	AD23	
TP_PCI_AD<24>	AL4	AD24	
TP_PCI_AD<25>	AV10	AD25	
TP_PCI_AD<26>	AL9	AD26	
TP_PCI_AD<27>	AN7	AD27	
TP_PCI_AD<28>	AK7	AD28	
TP_PCI_AD<29>	AN6	AD29	
TP_PCI_AD<30>	AH12	AD30	
TP_PCI_AD<31>	AN11	AD31	
TP_PCI_C_BE_L<0>	AV3	C/BE0*	
TP_PCI_C_BE_L<1>	AY6	C/BE1*	
TP_PCI_C_BE_L<2>	AP5	C/BE2*	
TP_PCI_C_BE_L<3>	AW10	C/BE3*	
PCI_INTA_L	AT8	PIRQA*	
PCI_INTB_L	AR4	PIRQB*	
PCI_INTC_L	AT11	PIRQC*	
PCI_INTD_L	BA5	PIRQD*	
PCI_REQ0_L	AP4	REQ0*	
PCI_REQ1_L	AW5	REQ1*/GPIO50	
PCI_REQ2_L	AY4	REQ2*/GPIO52	
PCI_REQ3_L	AH8	REQ3*/GPIO54	
PCH_PCI_GNT0_L	AK11	GNT0* (IPU)	
PCH_PCI_GNT1_L	AK6	GNT1*/GPIO51	
PCH_PCI_GNT2_L	BA9	GNT2*/GPIO53	
PCH_PCI_GNT3_L	AM3	GNT3*/GPIO55	
PCI_INTE_L	AU8	PIRQE*/GPIO2	
AUD_IP_PERIPHERAL_DET	AH7	PIRQF*/GPIO3	
PCI_INTG_L	AP12	PIRQG*/GPIO4	
AUD_I2C_INT_L	AW4	PIRQH*/GPIO5	
TP_PCI_RESET_L	AH10	PCIRST*	
PCI_SERR_L	AV6	SERR*	
PCI_PERR_L	AT4	PERR*	
PCI_IRDY_L	AP7	IRDY*	
TP_PCI_PAR	AP6	PAR	
PCI_DEVSEL_L	AT6	DEVSEL*	
PCI_FRAME_L	AL7	FRAME*	
PCI_PLOCK_L	AK12	PLOCK*	
PCI_STOP_L	AN8	STOP*	
PCI_TRDY_L	AL6	TRDY*	
TP_PCI_PME_L	AH11	PME* (IPU)	
PLT_RESET_L	AV34	PLTRST*	
LPC_CLK33M_SMC_R	AF6	CLKOUT_PCI0	
LPC_CLK33M_LPCPLUS_R	AD7	CLKOUT_PCI1	
TP_PCI_CLK33M_OUT2	AF9	CLKOUT_PCI2	
TP_PCI_CLK33M_OUT3	AD9	CLKOUT_PCI3	
PCH_CLK33M_PCIOUT	AD12	CLKOUT_PCI4	

=PP3V3_S0_PCH_GPIO

R2010	10K	5%	1/16W	MF-LF	402			
R2011	10K	5%	1/16W	MF-LF	402			
R2012	10K	5%	1/16W	MF-LF	402			
R2013	10K	5%	1/16W	MF-LF	402			
R2015	10K	5%	1/16W	MF-LF	402			
R2016	10K	5%	1/16W	MF-LF	402			
R2017	10K	5%	1/16W	MF-LF	402			
R2018	10K	5%	1/16W	MF-LF	402			
R2030	10K	5%	1/16W	MF-LF	402			
R2031	10K	5%	1/16W	MF-LF	402			
R2020	10K	5%	1/16W	MF-LF	402			
R2021	10K	5%	1/16W	MF-LF	402			
R2022	10K	5%	1/16W	MF-LF	402			
R2023	10K	5%	1/16W	MF-LF	402			
R2024	10K	5%	1/16W	MF-LF	402			
R2027	10K	5%	1/16W	MF-LF	402			
R2025	10K	5%	1/16W	MF-LF	402			
R2026	10K	5%	1/16W	MF-LF	402			

NVRAM

NV_CE0*	H36	TP_NV_CE_L<0>
NV_CE1*	H35	TP_NV_CE_L<1>
NV_CE2*	P32	TP_NV_CE_L<2>
NV_CE3*	E41	TP_NV_CE_L<3>
NV_DQS0	P36	TP_NV_DQS<0>
NV_DQS1	F40	TP_NV_DQS<1>
NV_DQ0/NV_IO0	T33	TP_NV_DQ<0>
NV_DQ1/NV_IO1	P35	TP_NV_DQ<1>
NV_DQ2/NV_IO2	T31	TP_NV_DQ<2>
NV_DQ3/NV_IO3	P33	TP_NV_DQ<3>
NV_DQ4/NV_IO4	M35	TP_NV_DQ<4>
NV_DQ5/NV_IO5	L33	TP_NV_DQ<5>
NV_DQ6/NV_IO6	M36	TP_NV_DQ<6>
NV_DQ7/NV_IO7	M34	TP_NV_DQ<7>
NV_DQ8/NV_IO8	M30	TP_NV_DQ<8>
NV_DQ9/NV_IO9	F36	TP_NV_DQ<9>
NV_DQ10/NV_IO10	H33	TP_NV_DQ<10>
NV_DQ11/NV_IO11	F37	TP_NV_DQ<11>
NV_DQ12/NV_IO12	E39	TP_NV_DQ<12>
NV_DQ13/NV_IO13	G33	TP_NV_DQ<13>
NV_DQ14/NV_IO14	D40	TP_NV_DQ<14>
NV_DQ15/NV_IO15	F33	TP_NV_DQ<15>
(IPD) NV_ALE	J34	PCH_NV_ALE
(IPD) NV_CLE	L35	PCH_NV_CLE
NV_RCOMP	L36	TP_NV_RCOMP
(IPU) NV_RB*	M32	TP_NV_RB_L
NV_WR0_RE*	J36	TP_NV_WR_RE_L<0>
NV_WR1_RE*	J35	TP_NV_WR_RE_L<1>
NV_WE_CK0*	M31	TP_NV_WE_CK_L<0>
NV_WE_CK1*	F38	TP_NV_WE_CK_L<1>

USB

NOTE: Internal pull-downs on all USB pins

(OPD) USBP0N	AW25	USB_HUB1_UP_N	USB HUB 1
(OPD) USBP0P	AY25	USB_HUB1_UP_P	
USBP1N	BA23	TP_USB_1N	Unused
USBP1P	AY24	TP_USB_1P	
(OPD) USBP2N	AW23	USB_BRCRYPT_N	Blu-ray transcript
USBP2P	AY22	USB_BRCRYPT_P	
USBP3N	AR22	TP_USB_3N	Unused
USBP3P	AP22	TP_USB_3P	
(OPD) USBP4N	AV21	USB_WM_N	WM
USBP4P	AY22	USB_WM_P	
USBP5N	AY20	TP_USB_5N	Unused
USBP5P	AW21	TP_USB_5P	
USBP6N	AK20	TP_USB_6N	Unused
USBP6P	AL20	TP_USB_6P	
USBP7N	AV20	TP_USB_7N	Unused
USBP7P	AW19	TP_USB_7P	
(OPD) USBP8N	BA19	USB_HUB2_UP_N	USB HUB 2
USBP8P	AY18	USB_HUB2_UP_P	
USBP9N	AM20	TP_USB_9N	Unused
USBP9P	AN20	TP_USB_9P	
USBP10N	AV17	TP_USB_10N	Unused
USBP10P	AV18	TP_USB_10P	
USBP11N	AR20	TP_USB_11N	Unused
USBP11P	AT20	TP_USB_11P	
USBP12N	AK18	TP_USB_12N	Unused
USBP12P	AL18	TP_USB_12P	
USBP13N	AY17	TP_USB_13N	Unused
USBP13P	BA16	TP_USB_13P	

USBRBIAS* AY15 — PCH_USB_RBIAS
USBRBIAS AV15 — TIE TRACES TOGETHER CLOSE TO PINS

R2070 22.6 1% 1/16W MF-LF 402 — PLACE THE RESISTOR CLOSE TO COMMON POINT

OC0*/GPIO59	AT31	PCH_GPIO59_OC0_L
OC1*/GPIO40	AT30	USB_HUB_SOFT_RESET_L
OC2*/GPIO41	AK28	PCH_GPIO41_OC2_L
OC3*/GPIO42	AP30	PCH_GPIO42_OC3_L
OC4*/GPIO43	AP31	PCH_GPIO43_OC4_L
OC5*/GPIO9	AL28	PCH_GPIO09_OC5_L
OC6*/GPIO10	AL30	PCH_GPIO10_OC6_L
OC7*/GPIO14	AM30	PCH_GPIO14_OC7_L

=PP3V3_S5_PCH_GPIO

R2060	10K	5%	1/16W	MF-LF	402			
NOSTUFF R2061	10K	5%	1/16W	MF-LF	402			
R2062	10K	5%	1/16W	MF-LF	402			
R2067	10K	5%	1/16W	MF-LF	402			
R2065	10K	5%	1/16W	MF-LF	402			
R2064	10K	5%	1/16W	MF-LF	402			
R2066	10K	5%	1/16W	MF-LF	402			

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

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PCH PCI/FLASHCACHE/USB

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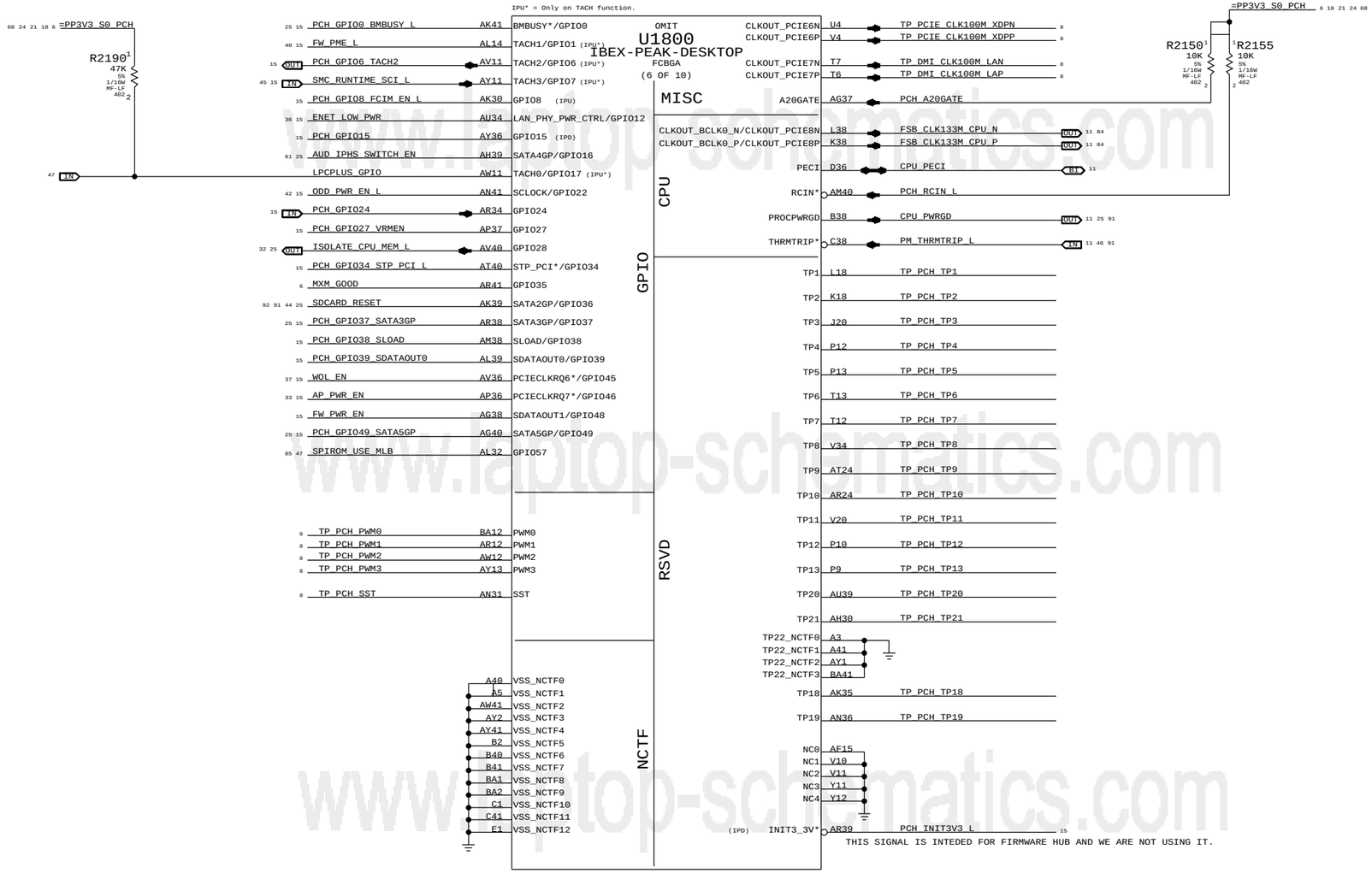

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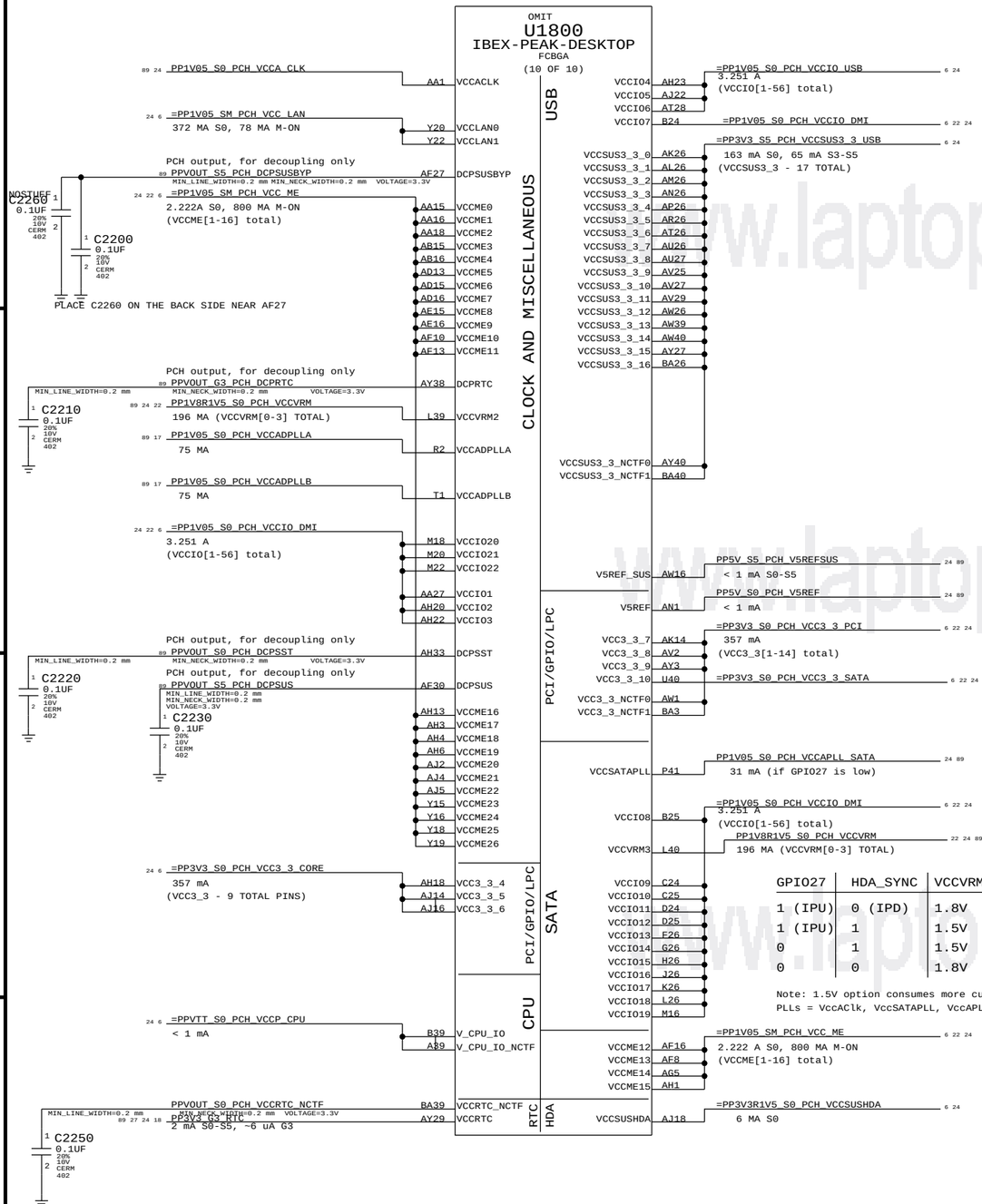

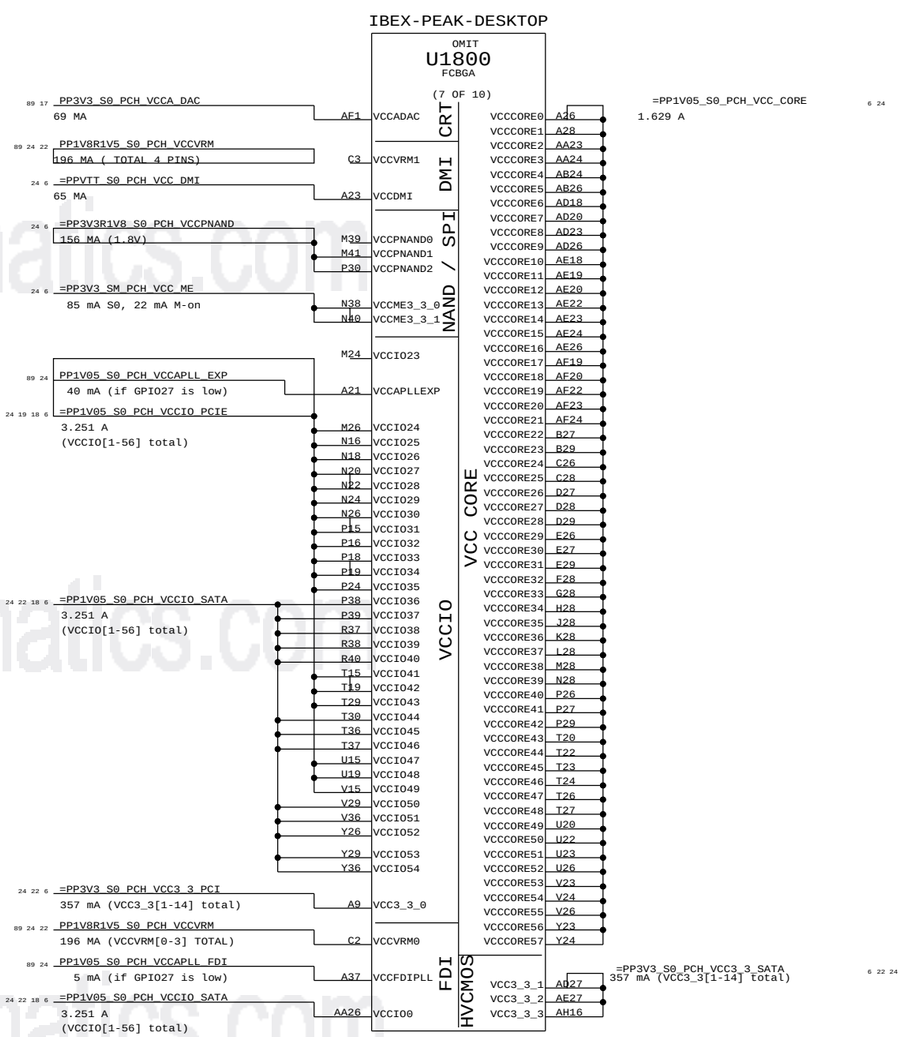

PAGE TITLE
PCH POWER

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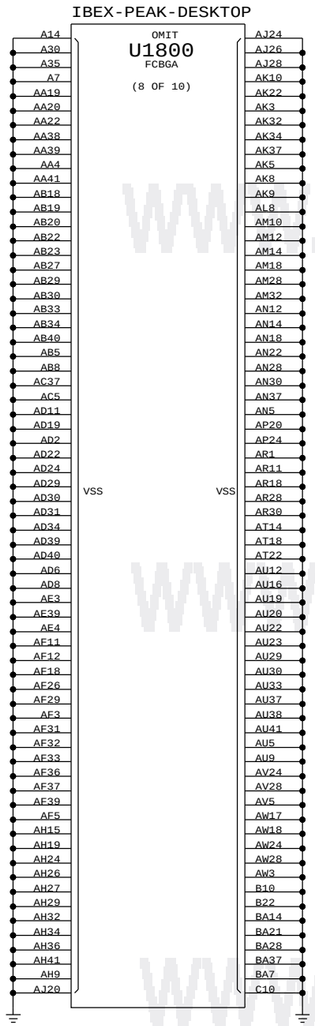

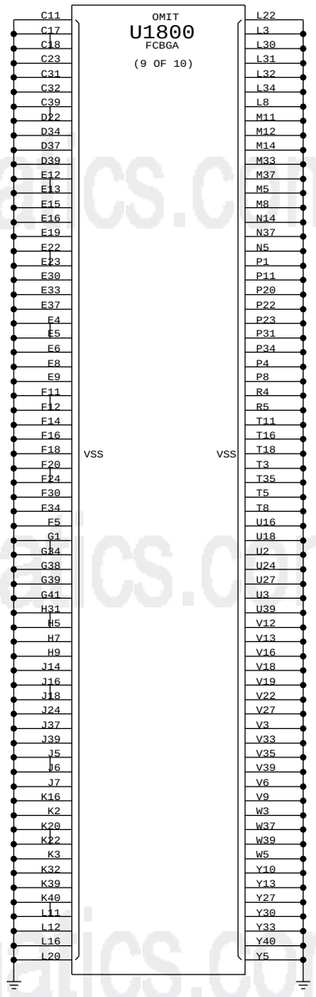

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PCH GROUNDS

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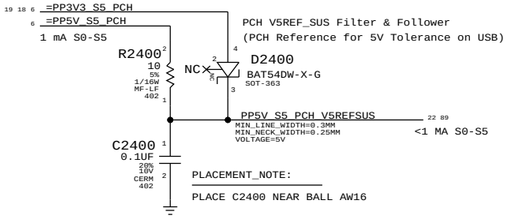
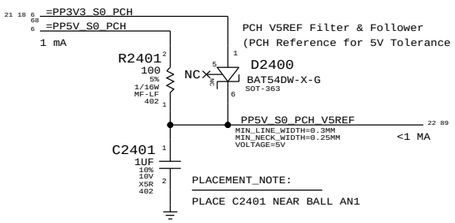
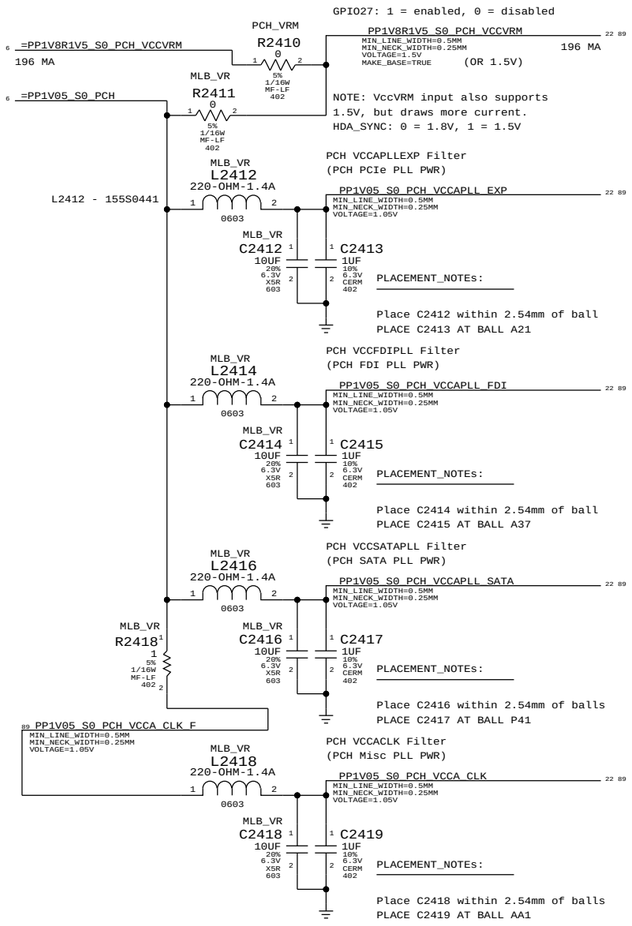
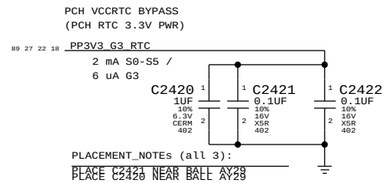
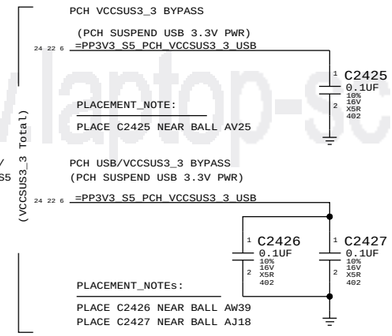


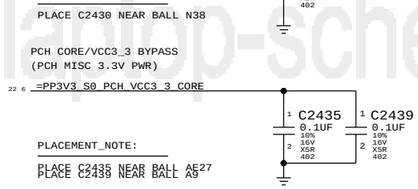


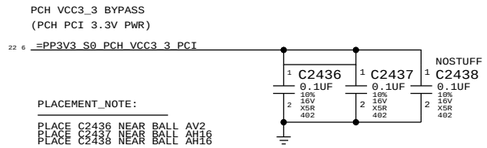


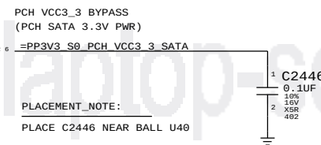
Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

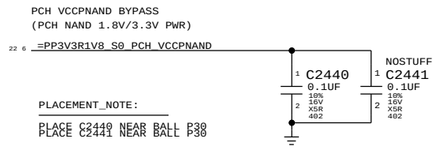


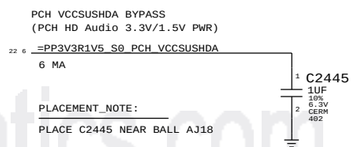


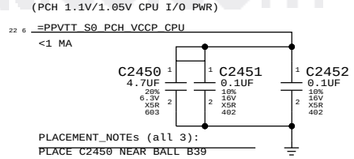


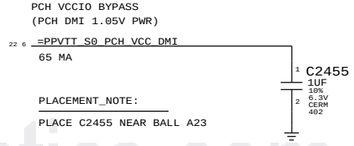


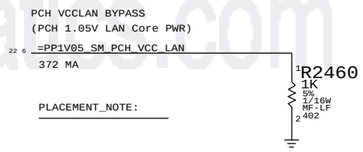


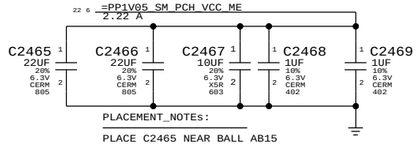


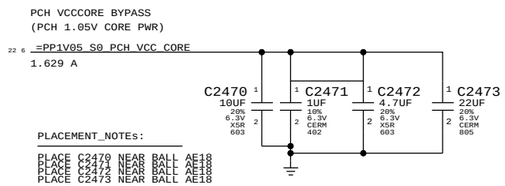


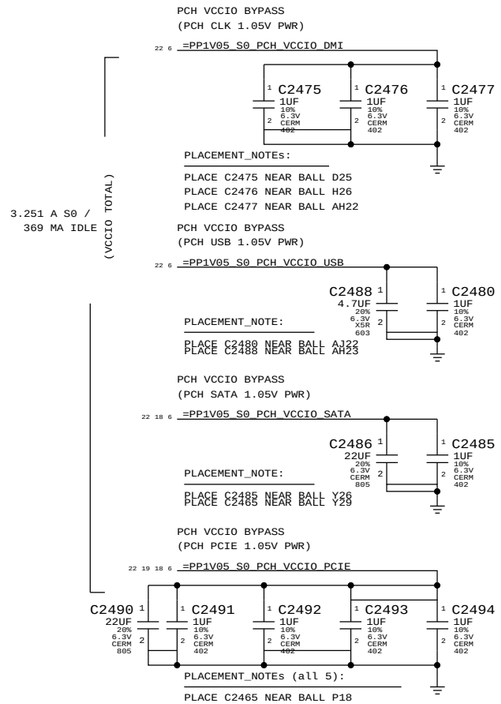












SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: PCH DECOUPLING

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D
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PAGE: 24 OF 110
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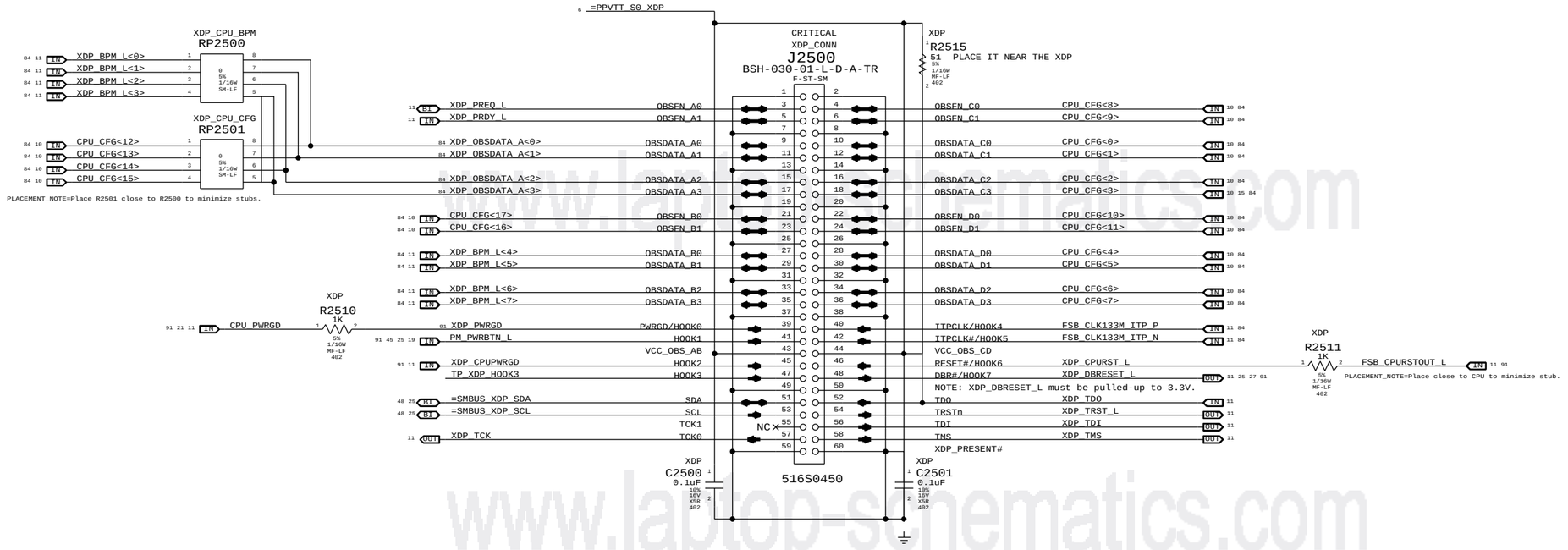
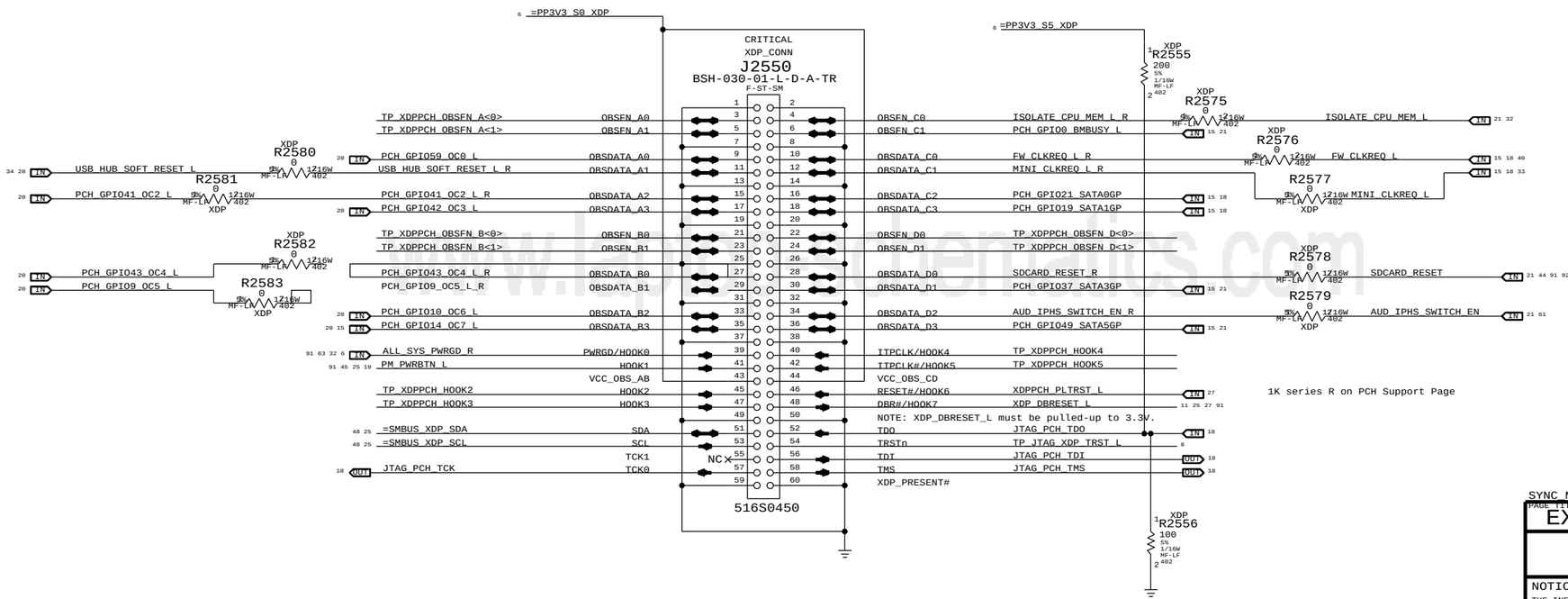
PROCESSOR XDP



PCH XDP



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE_TITLE
EXTENDED DEBUG PORT(XDP)

Apple Inc.

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REVISION A.0.0
BRANCH
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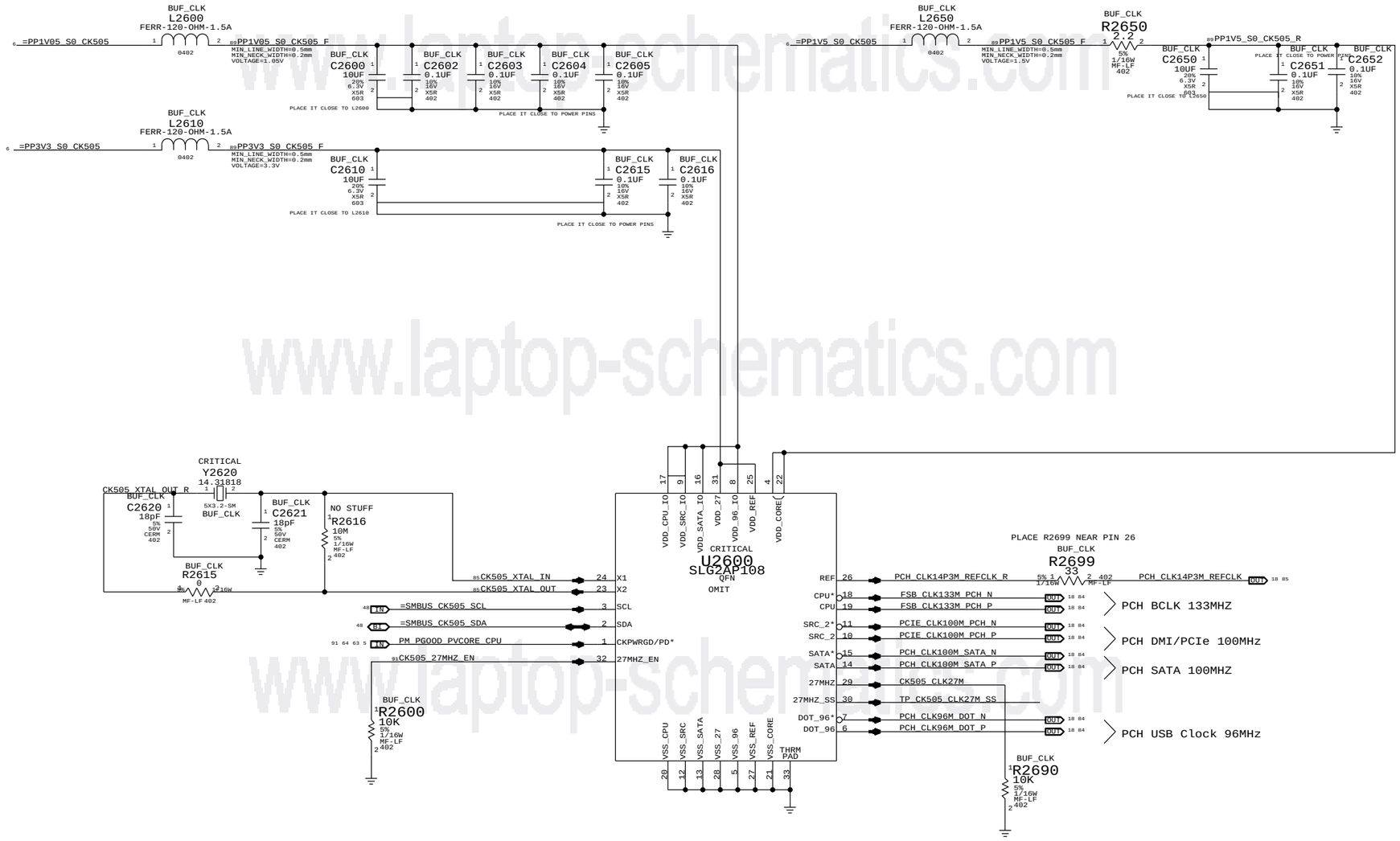

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: CLOCK (CK505)

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

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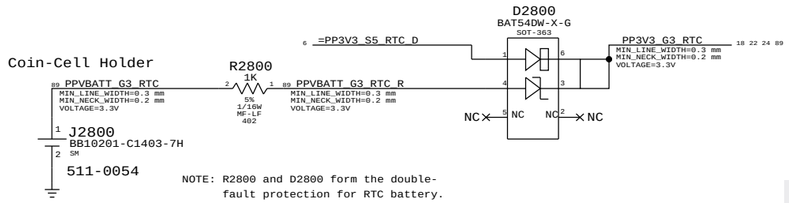
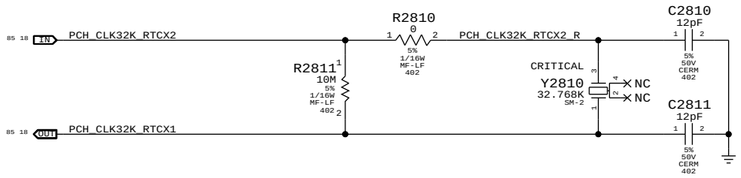
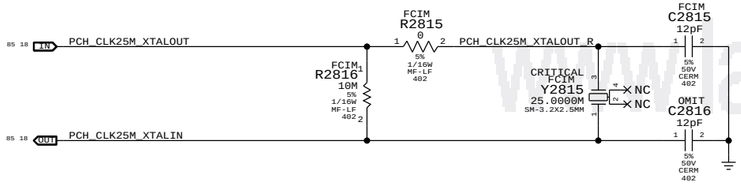
RTC Power Sources



PCH RTC Crystal



PCH 25MHz Crystal



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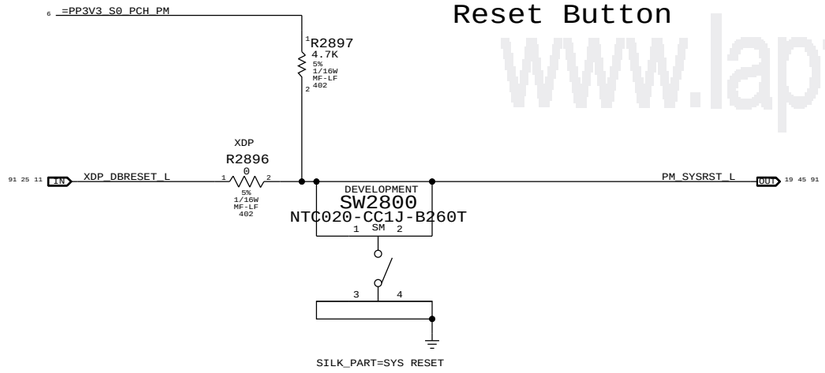
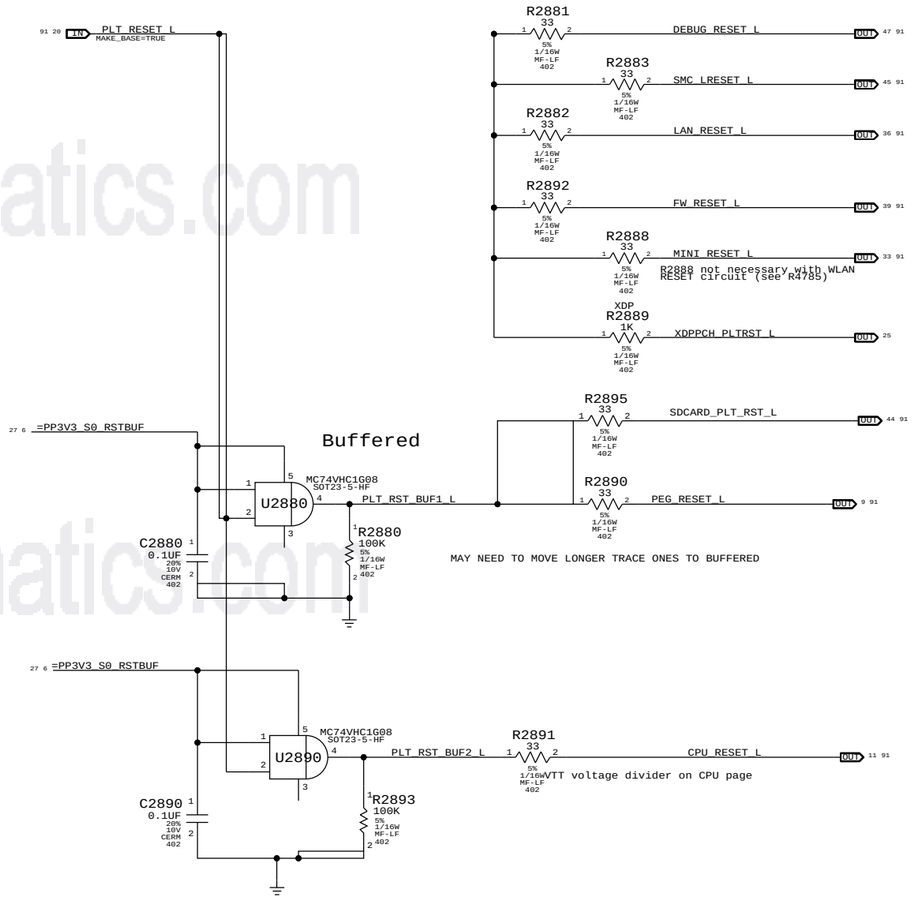
116S0004	1	RES,0,5%,0402	C2816	

Reset Button



Platform Reset Connections

Unbuffered



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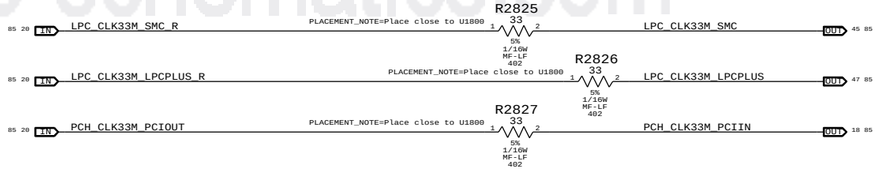

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

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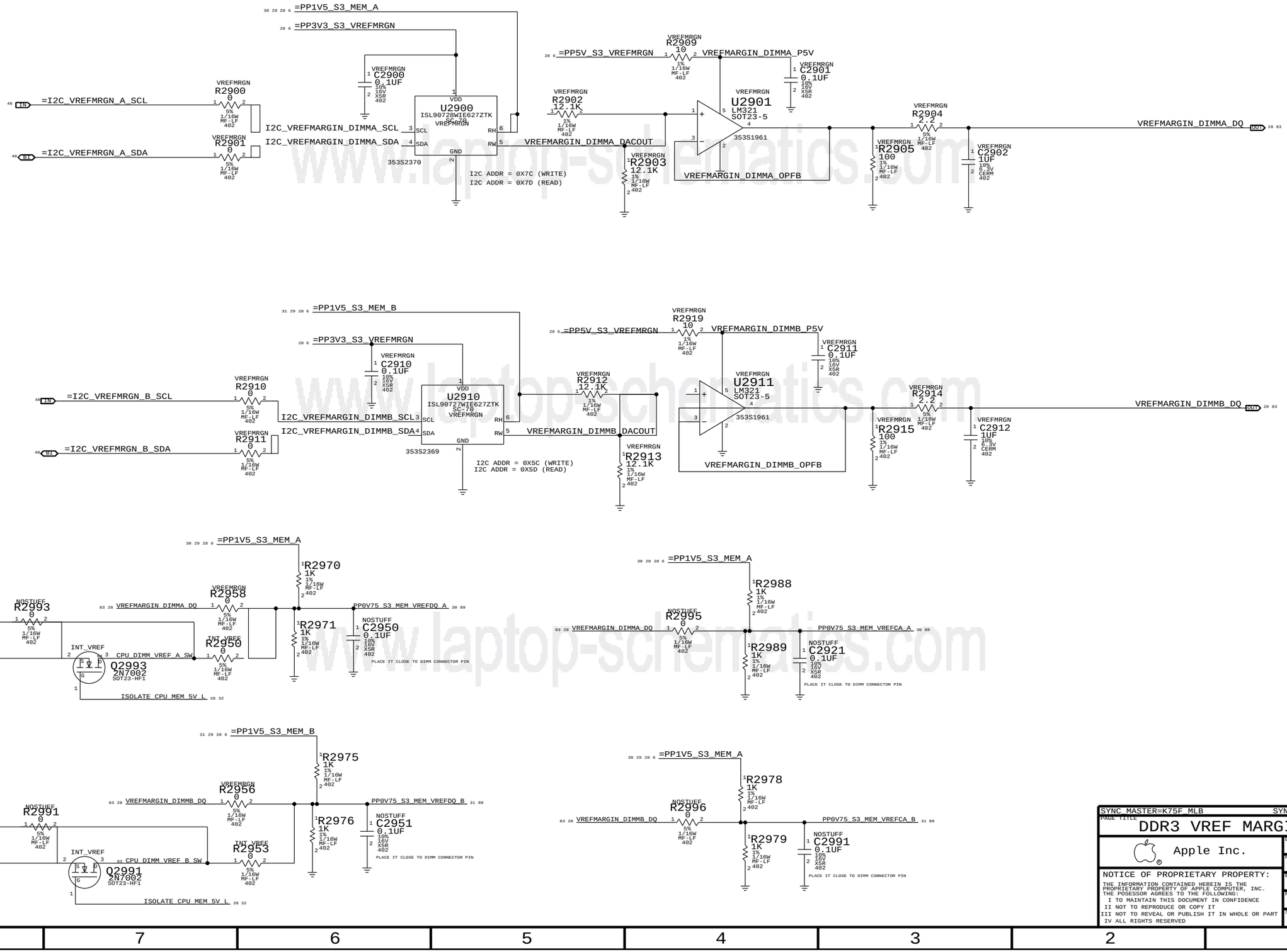

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

DDR3 VREF MARGINING

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DRAWING NUMBER 051-8600 SIZE D

REVISION A.0.0

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DIMM A (FURTHER FROM CPU) CAPS TO COUPLE CPU 1V5_MEM DIMM B (CLOSER TO CPU)

29 16 13 6 =PP1V5_CPU_MEM

C3016 1UF 10% 6.3V CERM 402
C3017 1UF 10% 6.3V CERM 402
C3018 1UF 10% 6.3V CERM 402
C3019 1UF 10% 6.3V CERM 402
C3010 1UF 10% 6.3V CERM 402
C3025 1UF 10% 6.3V CERM 402
C3026 1UF 10% 6.3V CERM 402
C3027 1UF 10% 6.3V CERM 402
C3028 1UF 10% 6.3V CERM 402
C3029 1UF 10% 6.3V CERM 402
C3020 1UF 10% 6.3V CERM 402
C3021 1UF 10% 6.3V CERM 402
C3022 1UF 10% 6.3V CERM 402
C3023 1UF 10% 6.3V CERM 402
C3014 1UF 10% 6.3V CERM 402
C3030 1UF 10% 6.3V CERM 402
C3031 1UF 10% 6.3V CERM 402
C3032 1UF 10% 6.3V CERM 402
C3033 1UF 10% 6.3V CERM 402

EXTRA DECOUPLING CAPS FOR CPU MEM RAIL

29 16 13 6 =PP1V5_CPU_MEM

C3041 1UF 10% 6.3V CERM 402
C3042 1UF 10% 6.3V CERM 402
C3044 1UF 10% 6.3V CERM 402
C3046 1UF 10% 6.3V CERM 402
C3040 1UF 10% 6.3V CERM 402
C3043 1UF 10% 6.3V CERM 402
C3045 1UF 10% 6.3V CERM 402
C3047 1UF 10% 6.3V CERM 402
C3048 1UF 10% 6.3V CERM 402
C3049 1UF 10% 6.3V CERM 402
C3090 1UF 10% 6.3V CERM 402
C3091 1UF 10% 6.3V CERM 402
C3092 1UF 10% 6.3V CERM 402
C3093 1UF 10% 6.3V CERM 402
C3094 1UF 10% 6.3V CERM 402

29 16 13 6 =PP1V5_CPU_MEM

C30A0 1UF 10% 6.3V CERM 402
C30A1 1UF 10% 6.3V CERM 402
C30A2 1UF 10% 6.3V CERM 402
C30A3 1UF 10% 6.3V CERM 402
C30A4 1UF 10% 6.3V CERM 402
C30A5 1UF 10% 6.3V CERM 402
C30A6 1UF 10% 6.3V CERM 402
C30A7 1UF 10% 6.3V CERM 402
C30A8 1UF 10% 6.3V CERM 402
C30A9 1UF 10% 6.3V CERM 402
C30AA 1UF 10% 6.3V CERM 402
C30AB 1UF 10% 6.3V CERM 402
C30AC 1UF 10% 6.3V CERM 402
C30AD 1UF 10% 6.3V CERM 402
C30AE 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR

30 28 6 =PP1V5_S3_MEM_A

C3050 10UF 20% 6.3V XSR 603
C3051 10UF 20% 6.3V XSR 603
C3052 1UF 10% 6.3V CERM 402
C3053 1UF 10% 6.3V CERM 402
C3054 1UF 10% 6.3V CERM 402
C3055 1UF 10% 6.3V CERM 402
C3056 1UF 10% 6.3V CERM 402
C3057 1UF 10% 6.3V CERM 402
C3058 1UF 10% 6.3V CERM 402
C3059 1UF 10% 6.3V CERM 402
C3060 1UF 10% 6.3V CERM 402
C3061 1UF 10% 6.3V CERM 402
C3062 1UF 10% 6.3V CERM 402
C3063 1UF 10% 6.3V CERM 402
C3064 1UF 10% 6.3V CERM 402
C3065 1UF 10% 6.3V CERM 402
C3066 1UF 10% 6.3V CERM 402
C3067 1UF 10% 6.3V CERM 402
C3068 1UF 10% 6.3V CERM 402
C3069 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR

31 28 6 =PP1V5_S3_MEM_B

C3070 10UF 20% 6.3V XSR 603
C3071 10UF 20% 6.3V XSR 603
C3072 1UF 10% 6.3V CERM 402
C3073 1UF 10% 6.3V CERM 402
C3074 1UF 10% 6.3V CERM 402
C3075 1UF 10% 6.3V CERM 402
C3076 1UF 10% 6.3V CERM 402
C3077 1UF 10% 6.3V CERM 402
C3078 1UF 10% 6.3V CERM 402
C3079 1UF 10% 6.3V CERM 402
C3080 1UF 10% 6.3V CERM 402
C3081 1UF 10% 6.3V CERM 402
C3082 1UF 10% 6.3V CERM 402
C3083 1UF 10% 6.3V CERM 402
C3084 1UF 10% 6.3V CERM 402
C3085 1UF 10% 6.3V CERM 402
C3086 1UF 10% 6.3V CERM 402
C3087 1UF 10% 6.3V CERM 402
C3088 1UF 10% 6.3V CERM 402
C3089 1UF 10% 6.3V CERM 402

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: MEMORY CAPS

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D
REVISION: A.0.0
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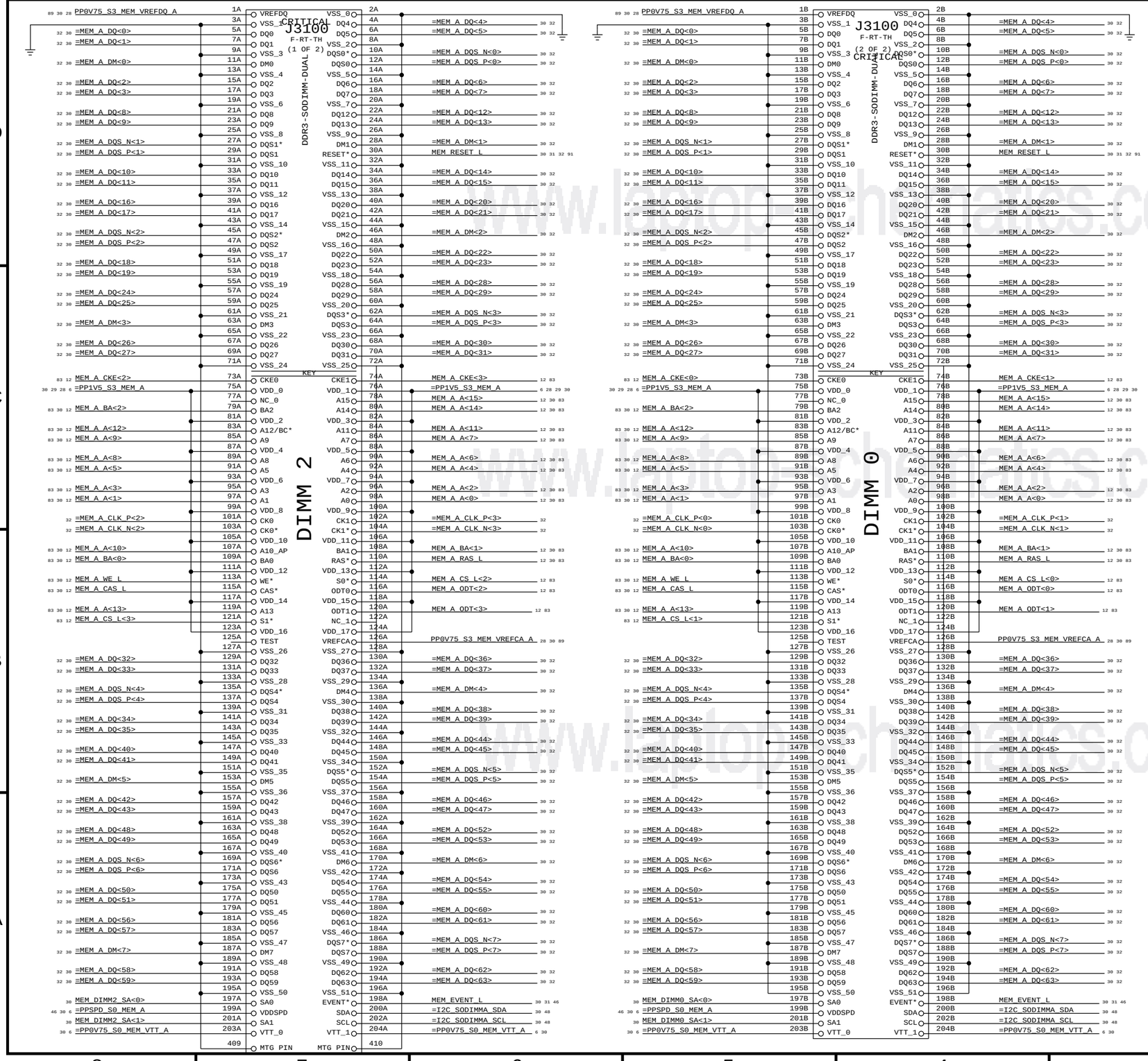

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: DDR3 SO-DIMMs 0 & 2

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DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

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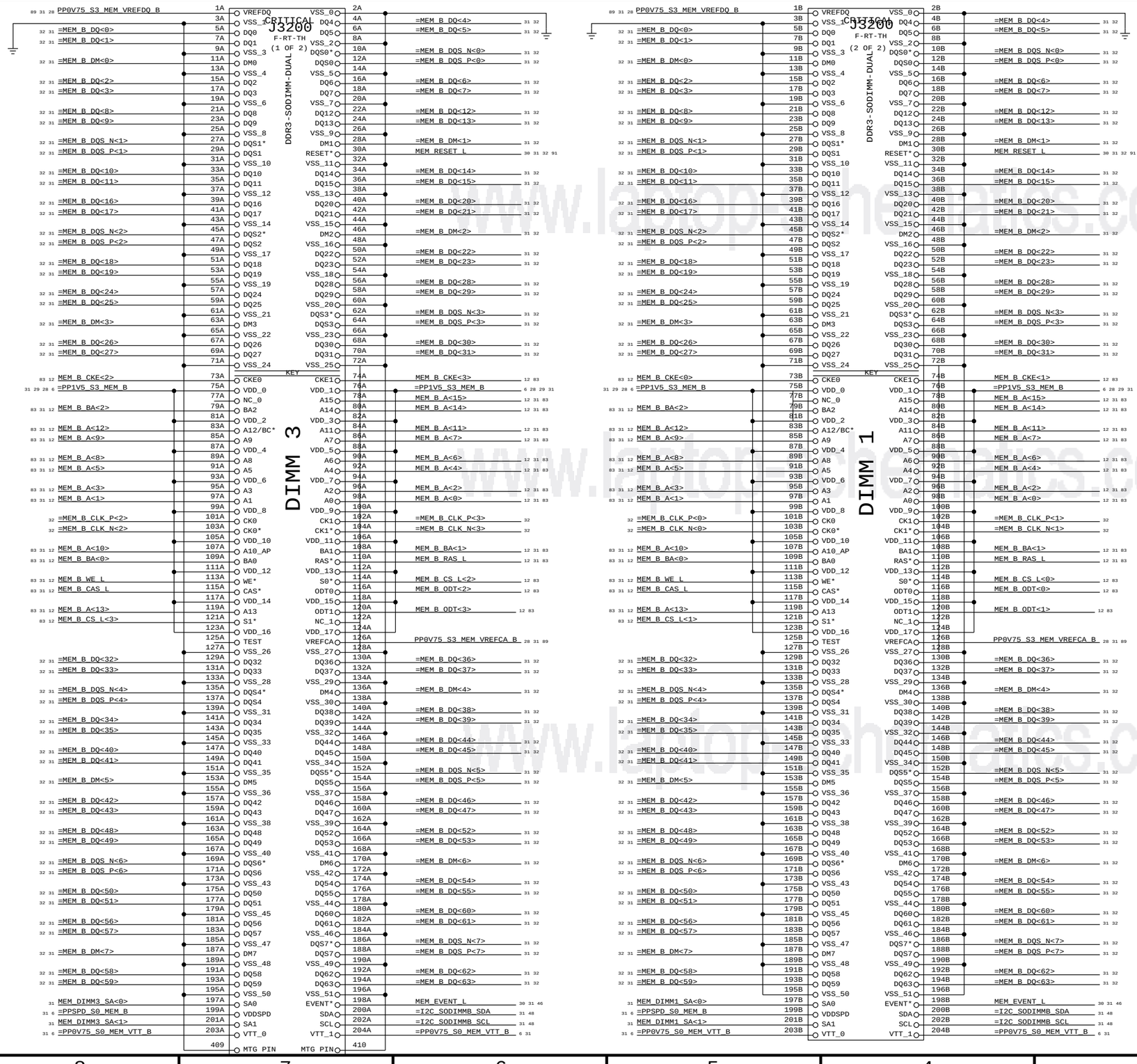

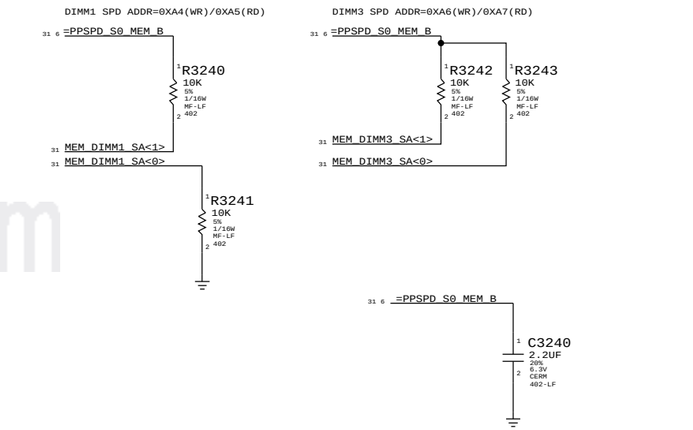

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA
- ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
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SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: DDR3 SO-DIMM CONNECTOR B

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DRAWING NUMBER: 051-8600 SIZE: D
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DDR3 RESET Support

LFD CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>
MEM_A_DM<0>	MAKE_BASE=TRUE	=MEM_A_DM<7>
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<57>
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<56>
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<58>
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<59>
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<60>
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<61>
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<62>
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<63>

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>
MEM_A_DM<1>	MAKE_BASE=TRUE	=MEM_A_DM<6>
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<49>
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<52>
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<51>
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<50>
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<48>
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<53>
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<55>
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<54>

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>
MEM_A_DM<2>	MAKE_BASE=TRUE	=MEM_A_DM<5>
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<40>
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<45>
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<46>
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<47>
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<41>
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<44>
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<43>
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<42>

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>
MEM_A_DM<3>	MAKE_BASE=TRUE	=MEM_A_DM<4>
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<37>
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<33>
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MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<34>
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<36>
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<32>
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<38>
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<39>

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>
MEM_A_DM<4>	MAKE_BASE=TRUE	=MEM_A_DM<3>
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<28>
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<29>
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<27>
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<31>
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<25>
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<24>
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<26>
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<30>

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>
MEM_A_DM<5>	MAKE_BASE=TRUE	=MEM_A_DM<2>
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<17>
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<16>
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<22>
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<23>
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<21>
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<20>
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<18>
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<19>

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>
MEM_A_DM<6>	MAKE_BASE=TRUE	=MEM_A_DM<1>
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<12>
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<13>
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<10>
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<15>
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<8>
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<9>
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<11>
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<14>

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>
MEM_A_DM<7>	MAKE_BASE=TRUE	=MEM_A_DM<0>
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<5>
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<4>
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<3>
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<2>
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<1>
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<0>
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<7>
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<6>

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>
MEM_B_DM<0>	MAKE_BASE=TRUE	=MEM_B_DM<7>
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<61>
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<60>
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<62>
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<63>
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<56>
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<57>
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<58>
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<59>

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>
MEM_B_DM<1>	MAKE_BASE=TRUE	=MEM_B_DM<6>
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<51>
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<54>
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<53>
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<52>
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<48>
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<49>
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<50>
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<55>

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>
MEM_B_DM<2>	MAKE_BASE=TRUE	=MEM_B_DM<5>
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<45>
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<40>
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<42>
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<47>
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<44>
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<41>
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<46>
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<43>

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>
MEM_B_DM<3>	MAKE_BASE=TRUE	=MEM_B_DM<4>
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<32>
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<39>
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<37>
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<38>
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<35>
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<34>
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<36>
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<33>

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>
MEM_B_DM<4>	MAKE_BASE=TRUE	=MEM_B_DM<3>
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<28>
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<24>
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<31>
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<30>
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<29>
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<25>
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<27>
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<26>

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>
MEM_B_DM<5>	MAKE_BASE=TRUE	=MEM_B_DM<2>
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<18>
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<20>
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<23>
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<22>
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<19>
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<21>
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<17>
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<16>

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>
MEM_B_DM<6>	MAKE_BASE=TRUE	=MEM_B_DM<1>
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<8>
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<14>
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<10>
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<11>
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<9>
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<15>
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<12>
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<13>

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>
MEM_B_DM<7>	MAKE_BASE=TRUE	=MEM_B_DM<0>
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<2>
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<1>
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<3>
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<7>
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<4>
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<5>
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<6>
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<0>

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE	=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	=MEM_A_CLK_N<1>
MEM_A_CLK_P<2>	MAKE_BASE=TRUE	=MEM_A_CLK_P<2>
MEM_A_CLK_N<2>	MAKE_BASE=TRUE	=MEM_A_CLK_N<2>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	=MEM_A_CLK_P<3>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	=MEM_A_CLK_N<3>
MEM_B_CLK_P<0>	MAKE_BASE=TRUE	=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	=MEM_B_CLK_N<1>
MEM_B_CLK_P<2>	MAKE_BASE=TRUE	=MEM_B_CLK_P<2>
MEM_B_CLK_N<2>	MAKE_BASE=TRUE	=MEM_B_CLK_N<2>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	=MEM_B_CLK_P<3>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	=MEM_B_CLK_N<3>

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: DDR3 SUPPORT AND BITSWAPS

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

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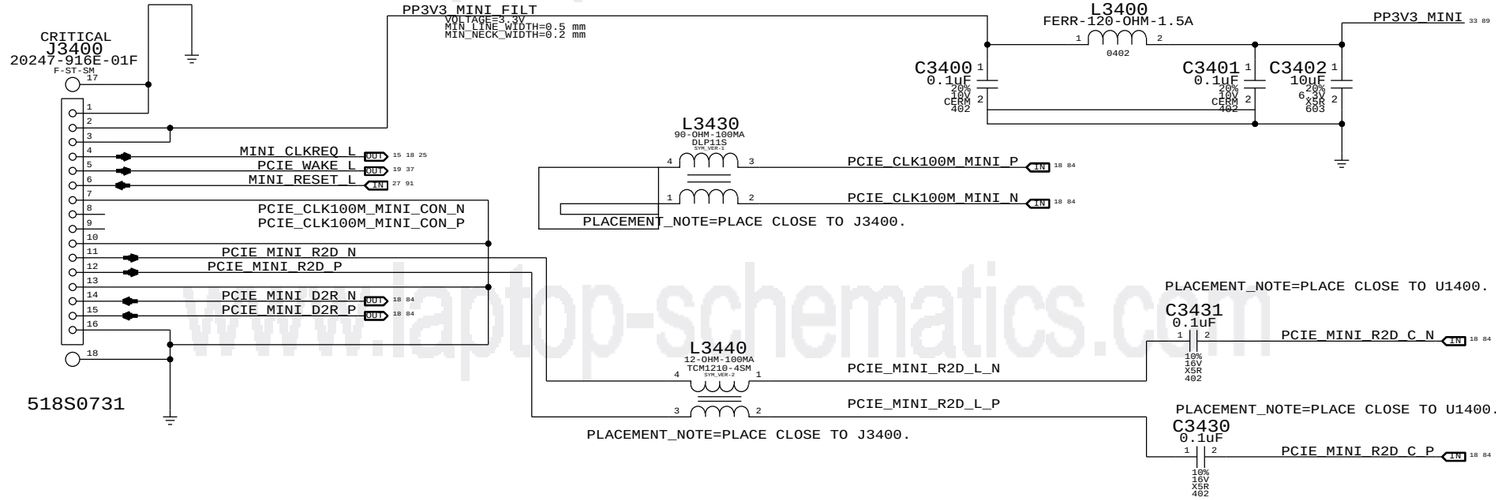
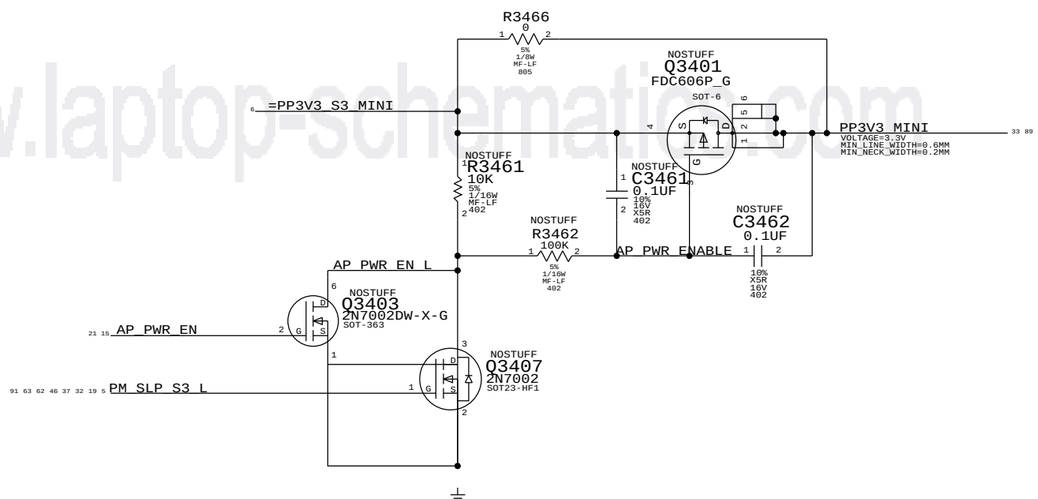


AP POWER ENABLE CIRCUIT

AP_PWR_ON = S0 || (S3 && AP_EN)



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

PCI-E Wireless Connector

Apple Inc.

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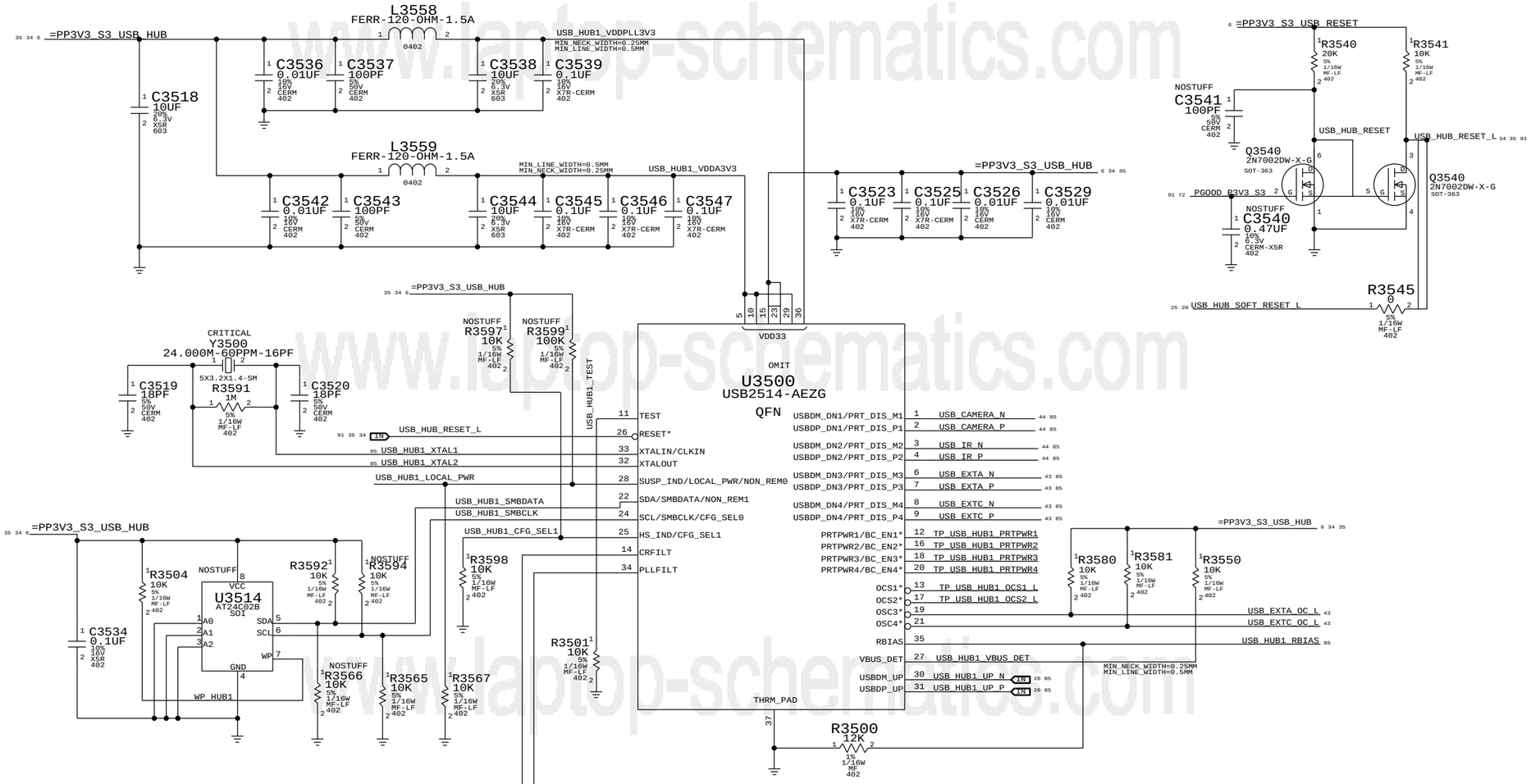
USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: USB HUB 1

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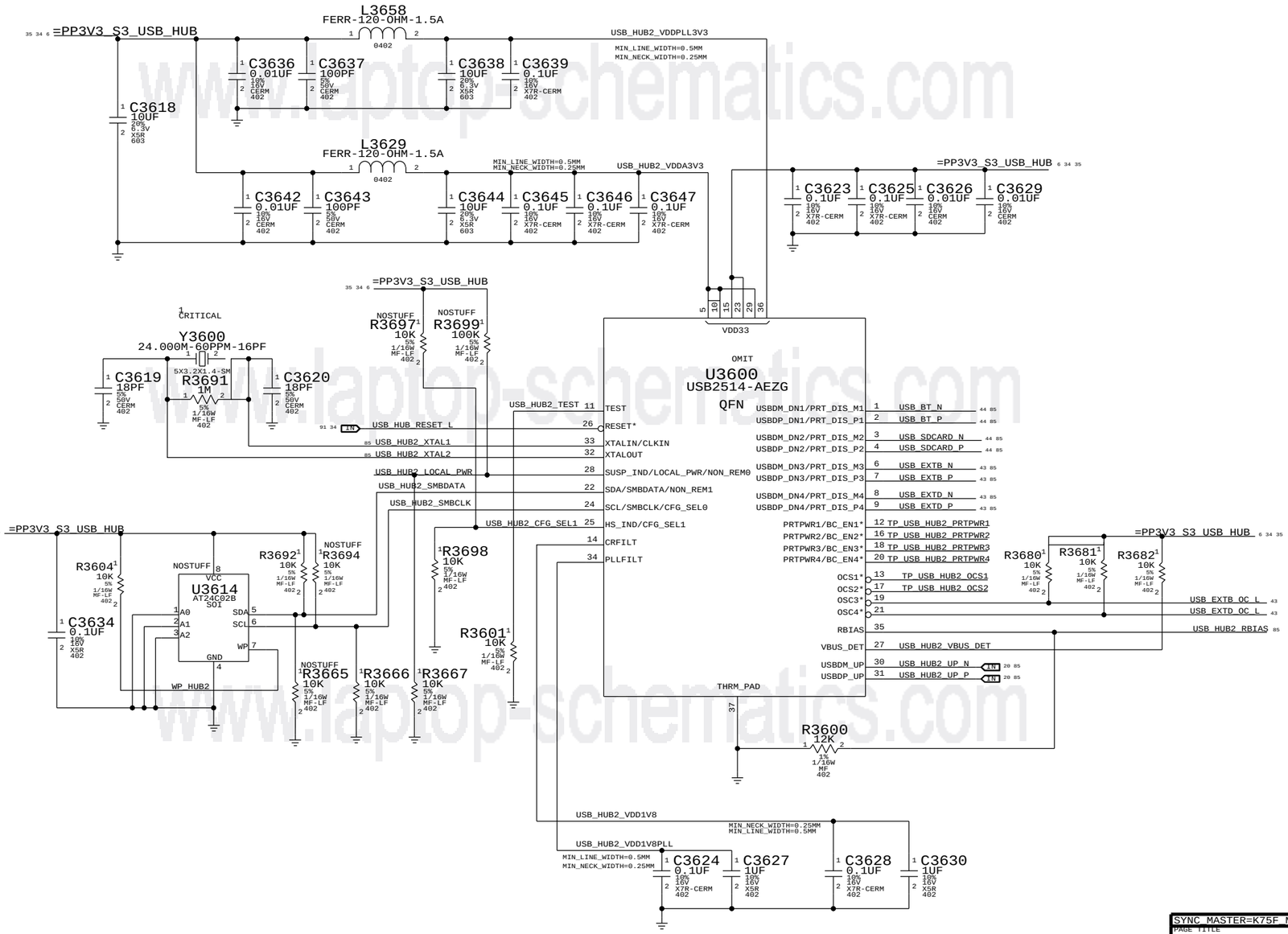
USB HUB-2



SYNC_MASTER=K75F_MLB	SYNC_DATE=04/14/2010
PAGE TITLE	USB HUB 2
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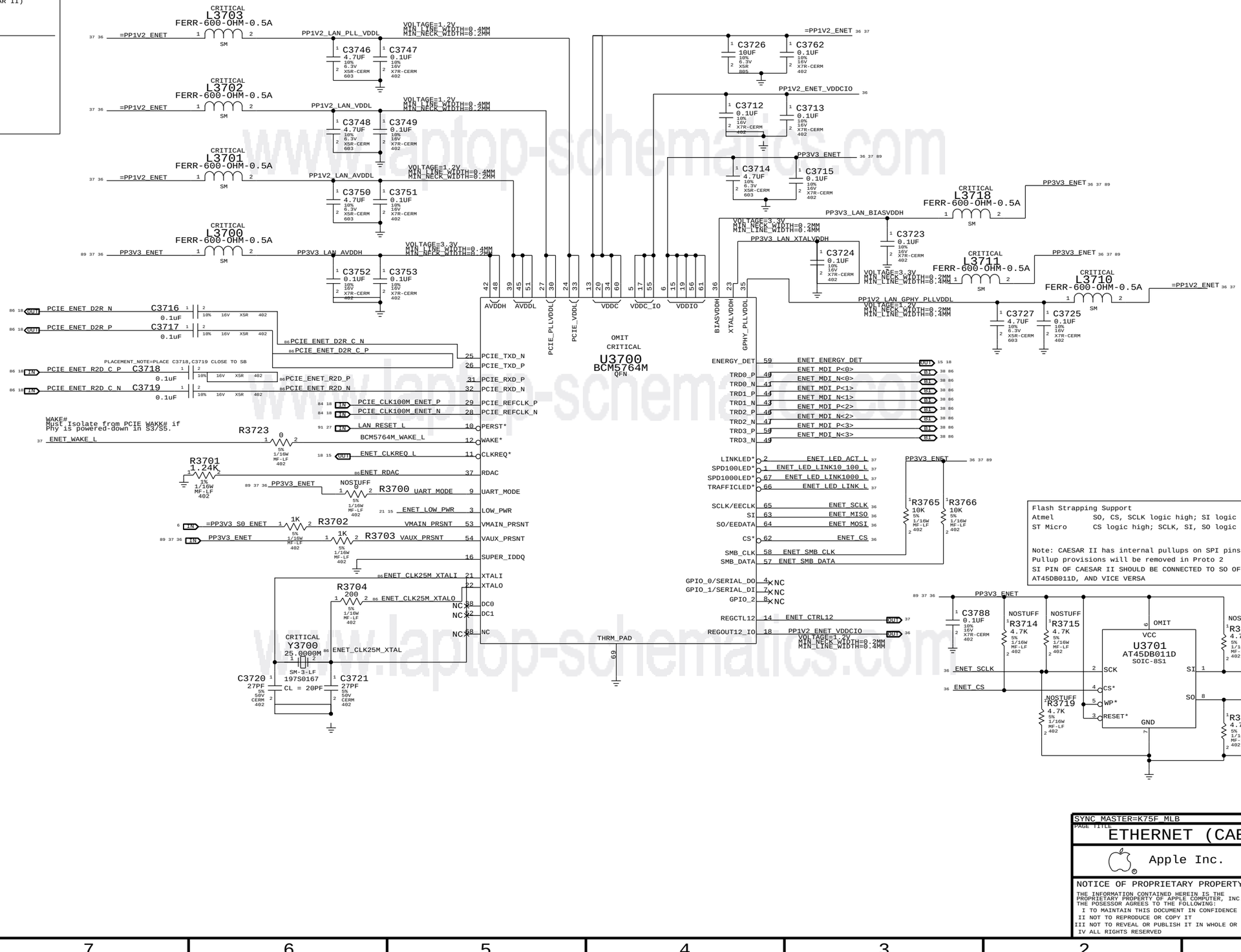
Page Notes

Power aliases required by this page:
- PP3V3_ENET (CAESAR II)
- =PP1V2_ENET



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: ETHERNET (CAESAR II)

Apple Inc.

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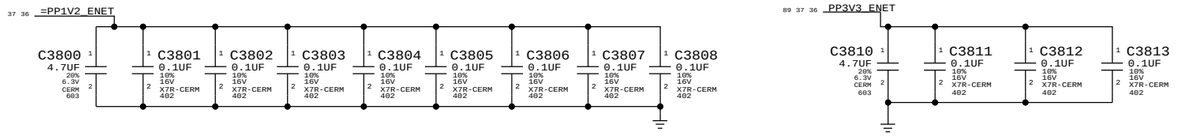
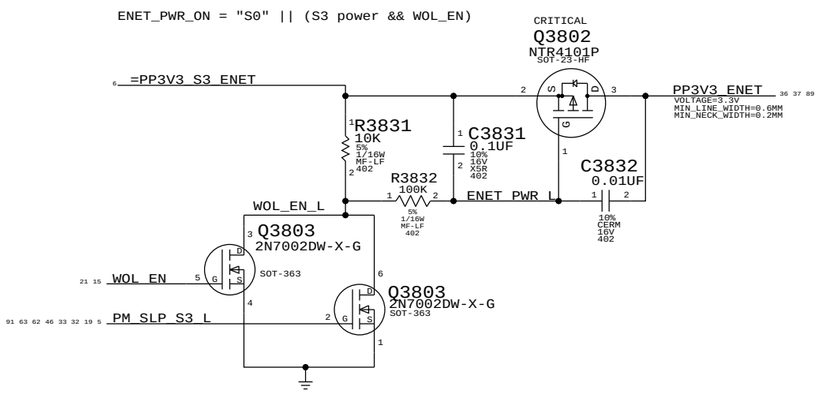
CAESAR II DECOUPLING

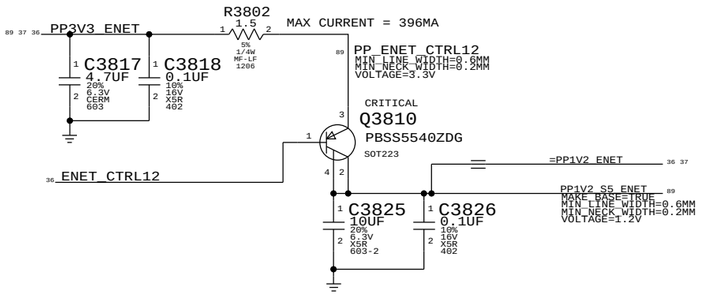


ENET POWER ENABLE CIRCUIT

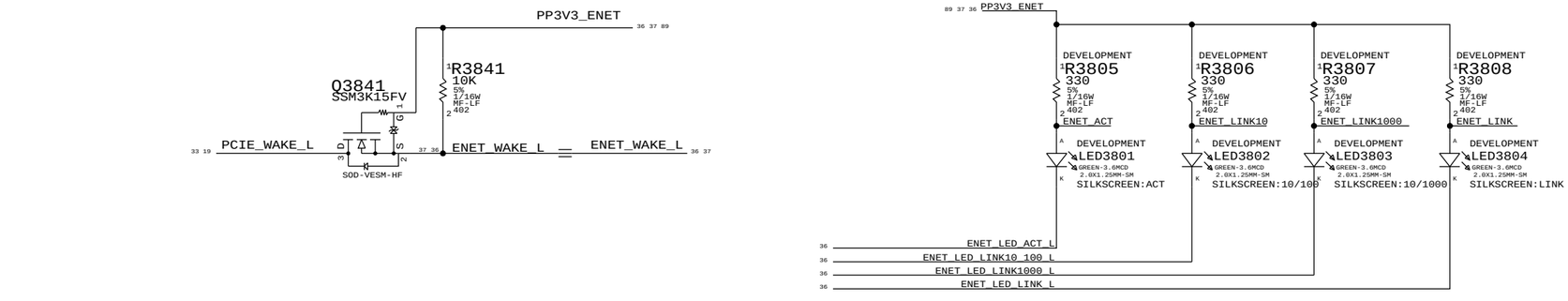
ENET_PWR_ON = "S0" || (S3 power && WOL_EN)



CAESAR II 1V2 RAIL SUPPLY



CAESAR II LED SUPPORT



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
CAESAR II SUPPORT

Apple Inc.

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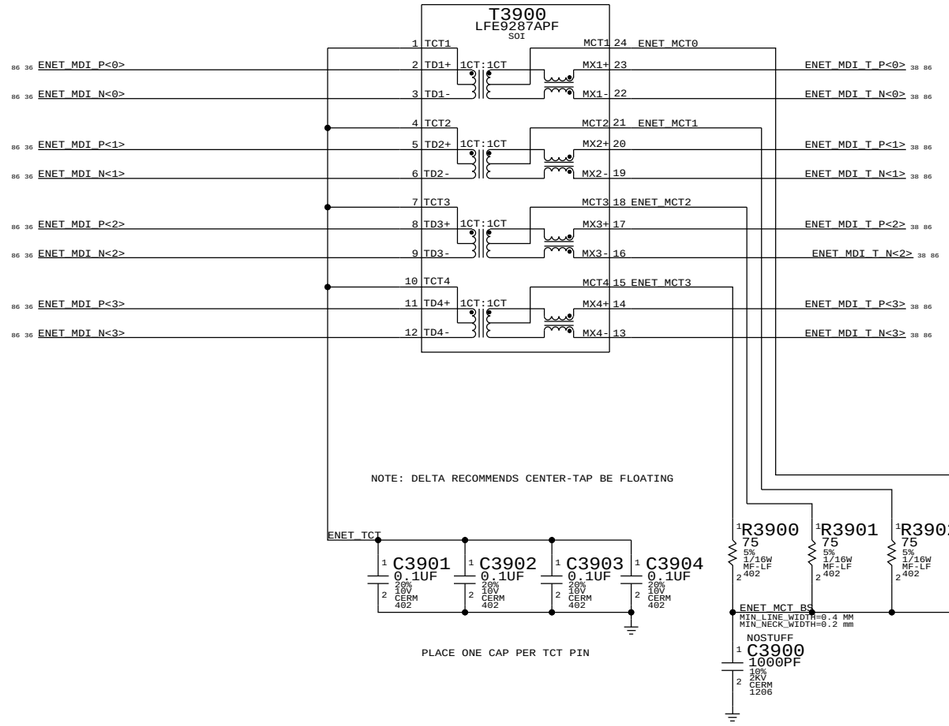

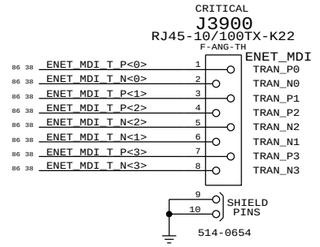

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

ETHERNET CONNECTOR

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Power Aliases:

FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.

FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.

For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.

PCI EXPRESS

1394B OHCI & PHY

Single-port:
PC[0:2] = '000'

Multiple-ports:
PC[0:2] = '100'

Alias =FWPHY_PC0 as appropriate

Unused Ports:

TP/NC TPBIASx
TP/NC TPAx_P/TPAx_N
Ground TPBx_P/TPBx_N

DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors

Strap DSx high on unused ports.

SYNC_MASTER=K75F_MLB	SYNC_DATE=04/14/2010
PAGE TITLE: FireWire LLC/PHY (XIO2213B)	
Apple Inc.	DRAWING NUMBER: 051-8600 SIZE: D
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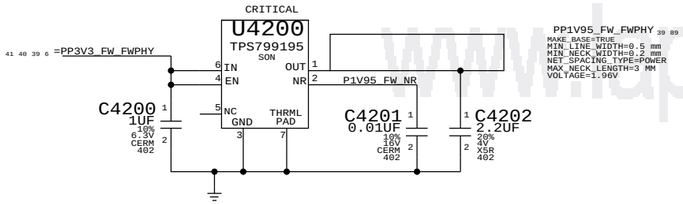
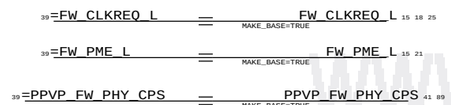
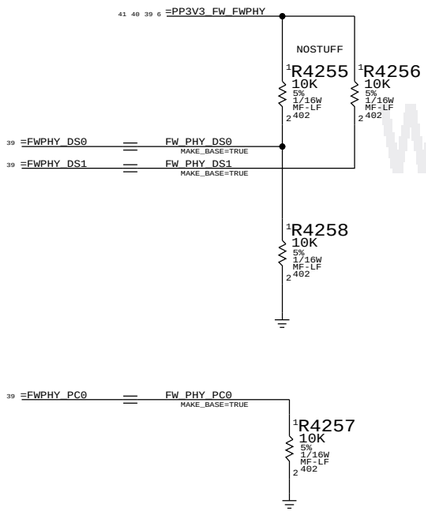
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity



1394 PHY STRAPPING OPTIONS

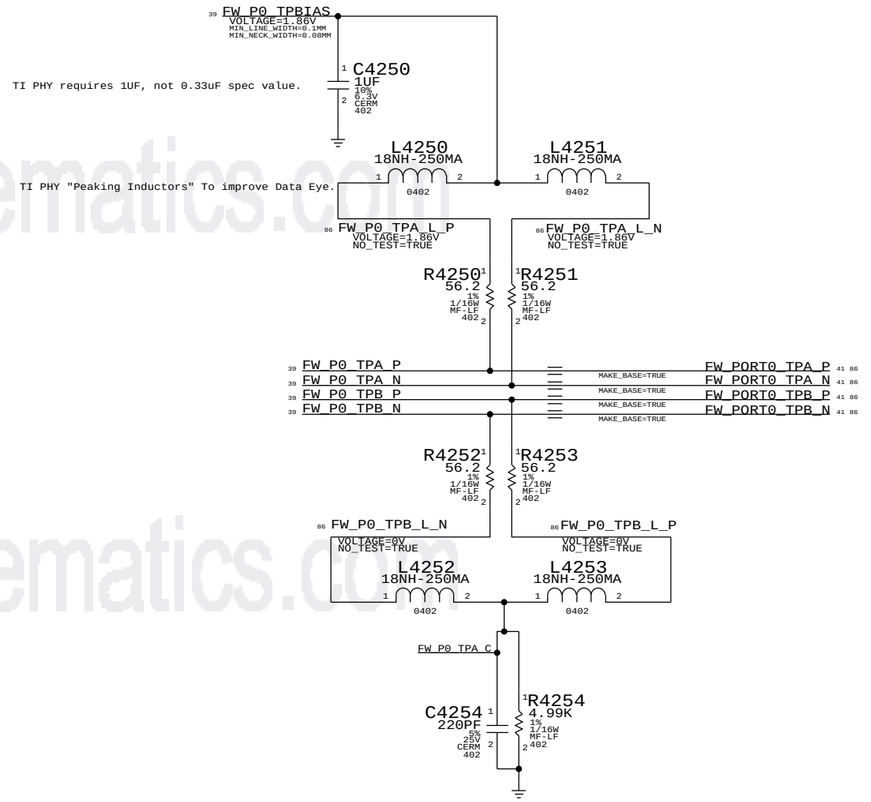


THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

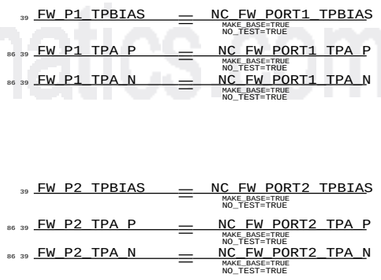
iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

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FW: 1394B MISC

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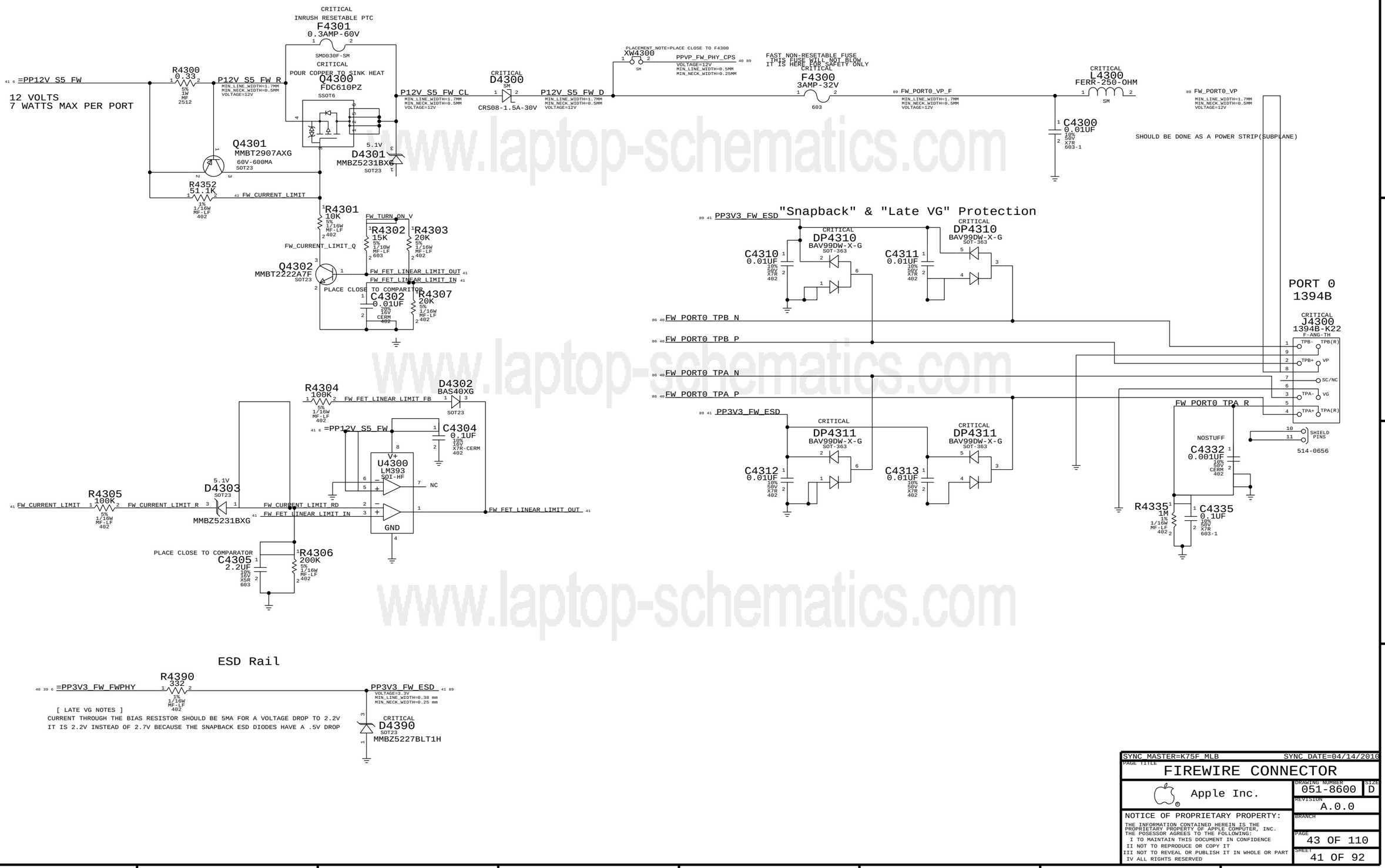

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D
REVISION A.0.0
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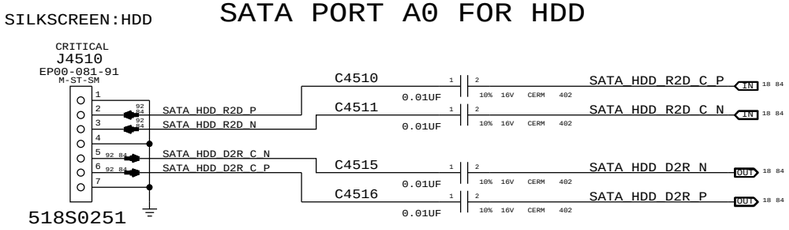
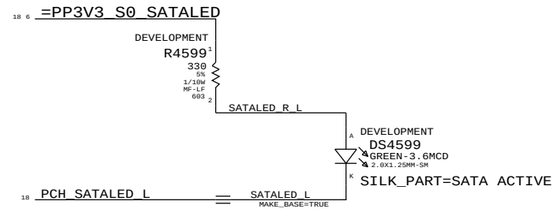
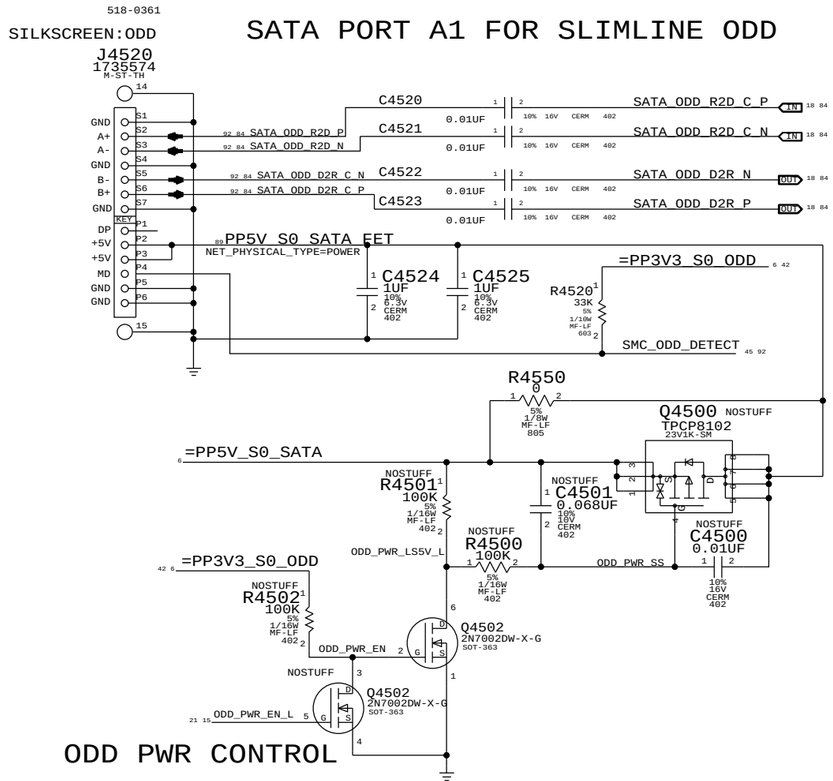
SATA PORT A0 FOR HDD



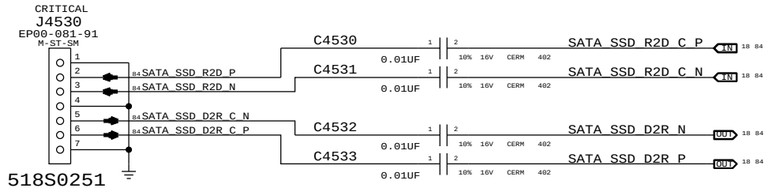
SATA Activity LED



SATA PORT A1 FOR SLIMLINE ODD



SATA PORT A2 FOR SSD



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: SATA Connectors

Apple Inc.

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USB/SMC DEBUG MUX

=PP3V3_G3H_SMCUSBMUX

=PP5V_S3_USB

U4601 TPS2060 MSOP

U4600 TPS2060 MSOP

U4650 PI3USB102ZLE TQFN

MOJOMUX

VCC

GND

SMC_RX_L

SMC_TX_L

USB_EXTD_P

USB_EXTD_N

USB_DEBUGPRT_EN_L

SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB

USB_EXTD_OC_L

USB_EXTA_OC_L

USB_EXTB_OC_L

USB_PWR_ENA_L

PM_EN_USB_PWR

Q4600 2N7002 SOT23-HF1

R4600 10K 5% 1/16W MF-LF 402

R4651 0 5% 1/16W MF-LF 402 PRODUCTION

R4652 0 5% 1/16W MF-LF 402 PRODUCTION

C4605 0.1UF 20% 10V CERM 402

C4606 330UF 20% 6.3V POLY-TANT CASE-D3L-SM CRITICAL

C4601 0.1UF 20% 10V CERM 402

C4602 330UF 20% 6.3V POLY-TANT CASE-D3L-SM CRITICAL

C4621 0.1UF 20% 10V CERM 402

C4631 0.1UF 20% 10V CERM 402

C4603 0.1UF 20% 10V CERM 402

C4611 0.1UF 20% 10V CERM 402

C4650 0.1UF 20% 10V CERM 402

C4630 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

C4610 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

C4620 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

C4600 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

L4630 FERR-250-OHM SM CRITICAL

L4631 120-OHM-90MA DLP0NS CRITICAL

L4621 120-OHM-90MA DLP0NS CRITICAL

L4610 FERR-250-OHM SM CRITICAL

L4611 120-OHM-90MA DLP0NS CRITICAL

L4620 FERR-250-OHM SM CRITICAL

L4600 FERR-250-OHM SM CRITICAL

L4601 120-OHM-90MA DLP0NS CRITICAL

PP5V_USB2_PORT3 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT3_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT1 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT1_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT2 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT2_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT0 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT0_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

USB_D_MUXED_N

USB_D_MUXED_P

USB_PORT3_N

USB_PORT3_P

USB_EXTC_N

USB_EXTC_P

USB_PORT2_N

USB_PORT2_P

USB_PORT1_N

USB_PORT1_P

USB_PORT0_N

USB_PORT0_P

USB_EXTB_N

USB_EXTB_P

USB_EXTA_N

USB_EXTA_P

J4630 USB-K22 F-ANG-TH CRITICAL 514-0659

J4620 USB-K22 F-ANG-TH CRITICAL 514-0659

J4610 USB-K22 F-ANG-TH CRITICAL 514-0672

J4600 USB-K22 F-ANG-TH CRITICAL 514-0672

D4630 RCLAMP0502N SLP1210N6 CRITICAL

D4620 RCLAMP0502N SLP1210N6 CRITICAL

D4610 RCLAMP0502N SLP1210N6 CRITICAL

D4600 RCLAMP0502N SLP1210N6 CRITICAL

VBUS DATA- DATA+ GND VDD D- D+

PORT 3

PORT 2

PORT 1

PORT 0

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: EXTERNAL USB CONNECTORS

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

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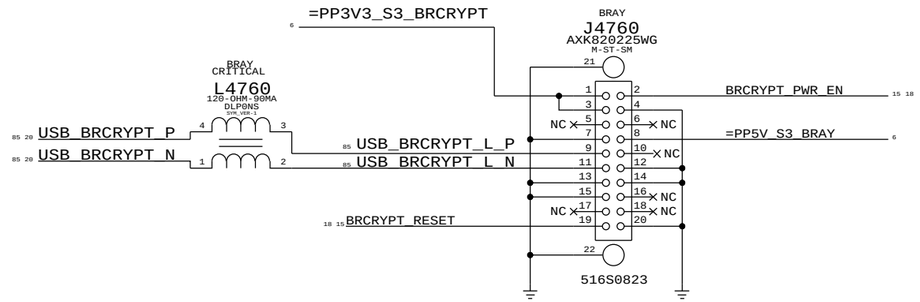
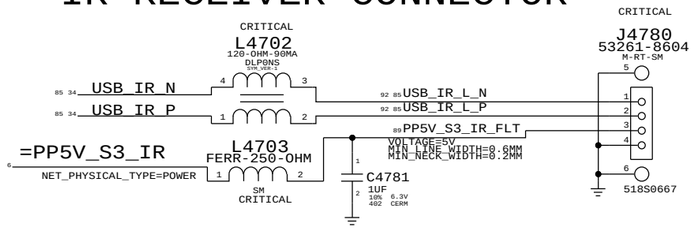
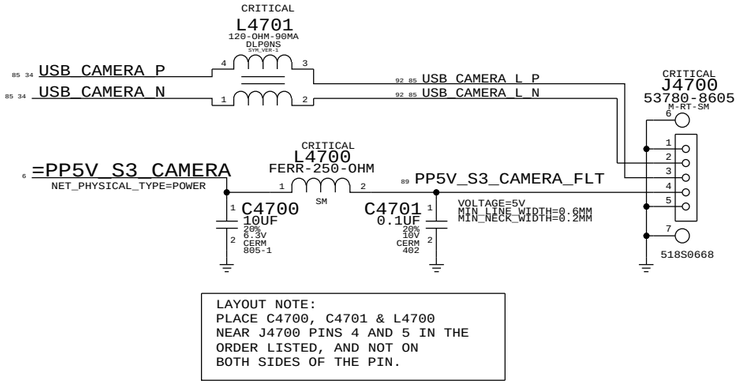
BLURAY DECRYPTOR CONN & FLTR



IR RECEIVER CONNECTOR

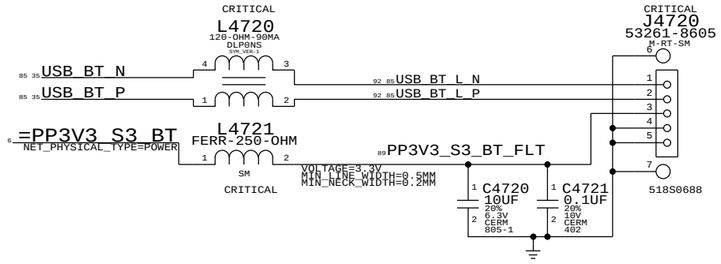


CAMERA CONNECTOR & FILTER

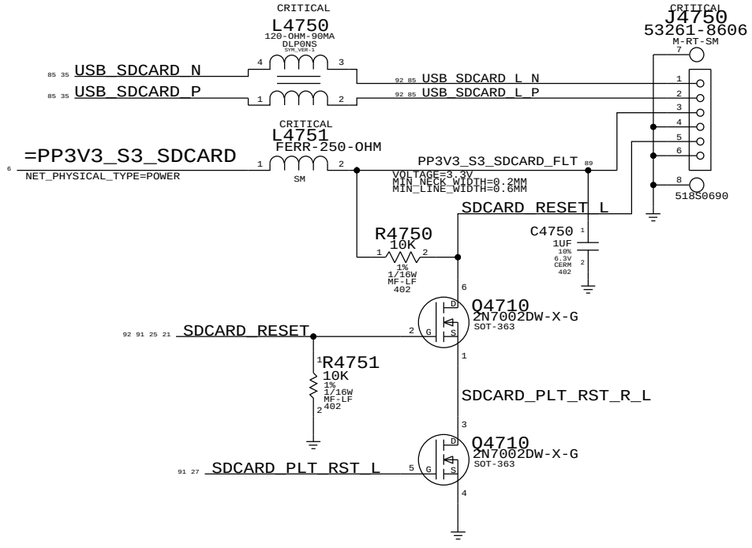


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

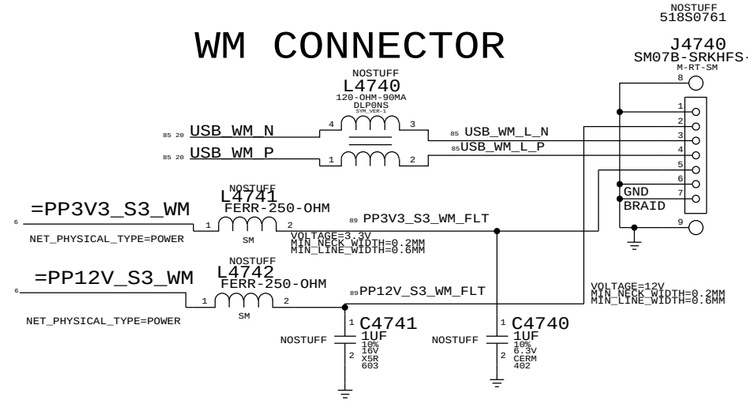
K37L (BLUETOOTH) CONNECTOR



SD Card Reader Board Connector



WM CONNECTOR



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Internal USB Connections

Apple Inc.

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

U4900
H8S2117
TQFP
(1 OF 3)
OMIT

46	OUT	SMC_EXCARD_PWR_EN	112	P10
46	OUT	SMC_RSTGATE_L	110	P11
91 63	IN	ALL_SYS_PWRGD_SMC	109	P12
91 63	IN	RSMRST_PWRGD	108	P13
	NC		107	P14
91 62	OUT	PM_RSMRST_L	106	P15
46	OUT	CPUIMVP_VR_ON	105	P16
91 25 19	OUT	PM_PWRBTN_L	104	P17
46	OUT	ESTARLDO_EN	103	P20
81	IN	SMC_VIDEO_ON	102	P21
81	IN	AUXCH_P_STATE	101	P22
81	IN	AUXCH_N_STATE	100	P23
	NC		99	P24
81	IN	SMC_DP_HPD	98	P25
81	OUT	BIDIVI_AUDIO_MUX_SEL	97	P26
81 78	OUT	DPMUX_VIDEO_IN_SEL	96	P27
85 47 18	BI	LPC_AD<0>	121	P30
85 47 18	BI	LPC_AD<1>	122	P31
85 47 18	BI	LPC_AD<2>	123	P32
85 47 18	BI	LPC_AD<3>	124	P33
85 47 18	IN	LPC_FRAME_L	125	P34
91 27	IN	SMC_LRESET_L	126	P35
85 27	IN	LPC_CLK33M_SMC	127	P36
47 18	BI	LPC_SERIRQ	128	P37
	NC		136	P40
46		SMC_P41	137	P41
48	BI	SMB_MGMT_DATA (OC)	138	P42
46	OUT	SMS_ONOFF_L	2	P43
	NC		3	P44
	NC		4	P45
46	OUT	SMC_GFX_THROTTLE_L	5	P46
	NC		6	P47
47 46 45 43	OUT	SMC_TX_L	16	P50
47 46 45 43	IN	SMC_RX_L	15	P51
48	BI	SMB_0_S0_CLK (OC)	14	P52

=PP3V3_G3H_SMC

Remove R4950,R4951 after Proto-1

NOSTUFF
R4951
10K
5%
1/16W
MF-LF
402

R4950
0
5%
1/16W
MF-LF
402

P60	78	SMC_PM_G2_R		SMC_PM_G2_EN OUT 3
P61	79	NC		
P62	80	NC		
P63	81	NC		
P64	82	SMC_ADAPTER_EN		OUT 19 46
P65	83	NC		
P66	84	SMC_PROCHOT_3_3_L		IN 46
P67	85	SMC_BIL_BUTTON_L		IN 46
P70	68	SMC_CPU_ISENSE		IN 49 88
P71	69	SMC_CPU_VSENSE		IN 49 88
P72	70	SMC_GPU_ISENSE		IN 50 88
P73	71	SMC_GPU_VSENSE		IN 50 88
P74	72	SMC_DCIN_ISENSE		IN 46
P75	73	SMC_PBUS_VSENSE		IN 46
P76	74	SMC_BATT_ISENSE		IN 46
P77	75	SMC_NB_MISC_ISENSE		IN 46
P80	129	SMC_WAKE_SCI_L		OUT 18
P81	130	NC		
P82	131	PM_CLKRUN_L		OUT 15 19 47 91
P83	132	LPC_PWRDWN_L		IN 19 47
P84	133	SMC_TX_L		OUT 43 45 46 47
P85	134	SMC_RX_L		IN 43 45 46 47
P86	135	(OC) SMB_MGMT_CLK		BI 48
P90	24	SMC_ONOFF_L		IN 46
P91	23	SMC_BC_ACOK		IN 46
P92	22	SMC_BS_ALRT_L		IN 46
P93	21	PM_SLPS3_BUF2_L		IN 6 46
P94	20	SMC_P94		
P95	19	PM_SLP_S4_S5		
P96	18	PM_CLK32K_SUSCLK		IN 9 85 91
P97	17	(OC) SMB_0_S0_DATA		BI 48

NOTE: P94 and P95 are shorted, P95 could be spare.

=PP3V3_G3H_SMC 6 45 46

NOSTUFF
R4952
10K
5%
1/16W
MF-LF
402

NOTE: Rename to BaseArch

R4954
0
5%
1/16W
MF-LF
402

PM_SLP_S4_2_L IN 19 46 91
PM_SLP_S5_L IN 19 91

NOSTUFF
R4953
0
5%
1/16W
MF-LF
402

R4955
0
5%
1/16W
MF-LF
402

REMOVE R4953/4/5 AFTER PROTO-1

PP3V3_G3H_AVREF_SMC 89 46 Peak/Ave/Standby = 2mA/1mA/5uA

=PP3V3_G3H_SMC 46 45 6 Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402

R4999
4.7
5%
1/16W
MF-LF
402

Peak/Ave/Standby= 2mA/1mA/5uA
PP3V3_G3H_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.4V

PLACEMENT_NOTE=Place C4907 close to U4900 pin 13

SMC_VCL

C4907 0.47UF 10% 6.3V CERM-XSR 402

C4920 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place R4999 close to U4900 pin 76
PLACEMENT_NOTE=Place C4920 close to U4900 pin 76

U4900
H8S2117
TQFP
(3 OF 3)
OMIT

76	AVCC			
1	VCC			
34	VCC			
56	VCC			
13	VCL			
77	AVREF			
91 47 46	IN	SMC_RESET_L	8	RES*
88 46		SMC_XTAL	143	XTAL
88 46		SMC_EXTAL	144	EXTAL
			MD1	9
			MD2	25
			NMI	11
			ETRST*	27
			AVSS	67
			VSS	7
			VSS	42
			VSS	95
			VSS	111
			VSS	139

R4909 10K 5% 1/16W MF-LF 402
R4901 10K 5% 1/16W MF-LF 402
R4902 10K 5% 1/16W MF-LF 402
R4998 10K 5% 1/16W MF-LF 402
R4903 0 5% 1/16W MF-LF 402

SMC_MD1 IN 47
SMC_KBC_MDE
SMC_NMI IN 47
SMC_TRST_L IN 47

XW4900
SM

GND_SMC_AVSS 46 49 50 88

U4900
H8S2117
TQFP
(2 OF 3)
OMIT

(DEBUG_SW_1)				
(DEBUG_SW_2)	46	SMC_PA0	41	PA0
18 15	OUT	SPI_DESCRIPTOR_OVERRIDE_L (OC)	40	PA1
91 27 19	OUT	PM_SYSRST_L (OC)	39	PA2
46 43	OUT	USB_DEBUGPRT_EN_L (OC)	38	PA3
46	IN	MEM_EVENT_A_L (OC)	37	PA4
46	IN	MEM_EVENT_B_L (OC)	35	PA5
46	BI	SYS_ONEWIRE (OC)	34	PA6
91 19 15	OUT	PM_BATLOW_L (OC)	33	PA7
	NC		120	PB0
21 18	OUT	SMC_RUNTIME_SCI_L	119	PB1
92 42	IN	SMC_ODD_DETECT	118	PB2
46		SMC_PB3 (See below)	117	PB3
51	IN	SMC_EXCARD_CP	116	PB4
	NC		115	PB5
46	IN	SMC_EXCARD_OC_L	114	PB6
46	IN	SMC_GFX_OVERTEMP_L	113	PB7
52	OUT	SMC_FAN_0_CTL	94	PC0
52	OUT	SMC_FAN_1_CTL	93	PC1
53	OUT	SMC_FAN_2_CTL	92	PC2
46	OUT	SMC_FAN_3_CTL	91	PC3
52	IN	SMC_FAN_0_TACH	90	PC4
52	IN	SMC_FAN_1_TACH	89	PC5
53	IN	SMC_FAN_2_TACH	88	PC6
46	IN	SMC_FAN_3_TACH	87	PC7
46	IN	SMS_X_AXIS	66	PD0
46	IN	SMS_Y_AXIS	65	PD1
46	IN	SMS_Z_AXIS	64	PD2
46	IN	SMC_ANALOG_ID	63	PD3
46	IN	SMC_NB_CORE_ISENSE	62	PD4
46	IN	SMC_NB_DDR_ISENSE	61	PD5
46	IN	ALS_LEFT	60	PD6
46	IN	ALS_RIGHT	59	PD7

PE0	32	SMC_CASE_OPEN		IN 46
PE1*	31	SMC_TCK		IN 46 47
PE2*	30	SMC_TDI		IN 46 47
PE3*	29	SMC_TDO		OUT 46 47
PE4*	28	SMC_TMS		IN 46 47
PF0	50	G3_POWERON_L		IN 46
PF1	49	SMC_SYS_LED		OUT 46
PF2	48	SMC_LID		OUT 46
PF3	47	BIDIVI_AUX_TERM_EN		OUT 81
PF4	46	BIDIVI_PNL_PWR_EN		OUT 81
PF5	45	SMC_PF5	46	
PF6	44	BIDIVI_BKL_ON		OUT 81
PF7	43	BIDIVI_BKL_PWM		OUT 81
PG0	58	SMC_PNL_BL_PWM		IN 46 81
PG1	57	=SMC_SMS_INT		IN 46
PG2	56	(OC) SMB_BSA_DATA		BI 48
PG3	55	(OC) SMB_BSA_CLK		BI 48
PG4	54	(OC) SMB_A_S3_DATA		BI 48
PG5	53	(OC) SMB_A_S3_CLK		BI 48
PG6	52	(OC) SMB_B_S0_DATA		BI 48
PG7	51	(OC) SMB_B_S0_CLK		BI 48
PH0	10	SMC_PROCHOT		OUT 46
PH1	12	SMC_THRMTRIP		OUT 46
PH2	26	SMC_PH2	46	
PH3	140	ALS_GAIN		OUT 46
PH4	141	NC		
PH5	142	NC		

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: SMC

Apple Inc.

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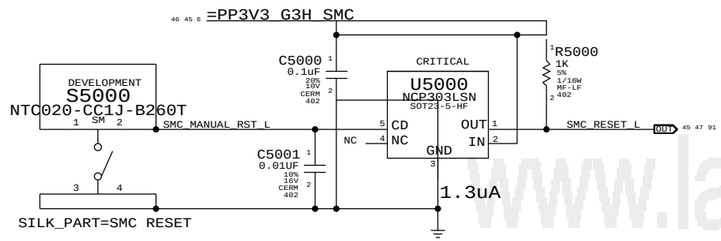
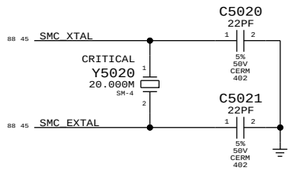
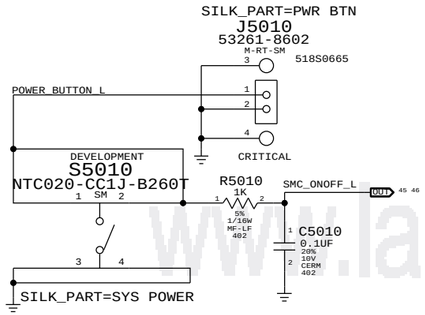
SMC Reset Button / Brownout Detect



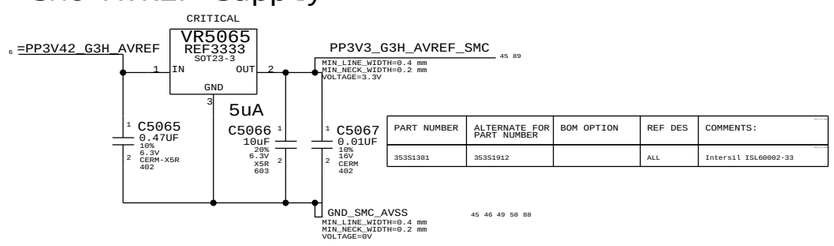
SMC Crystal Circuit



POWER BUTTON

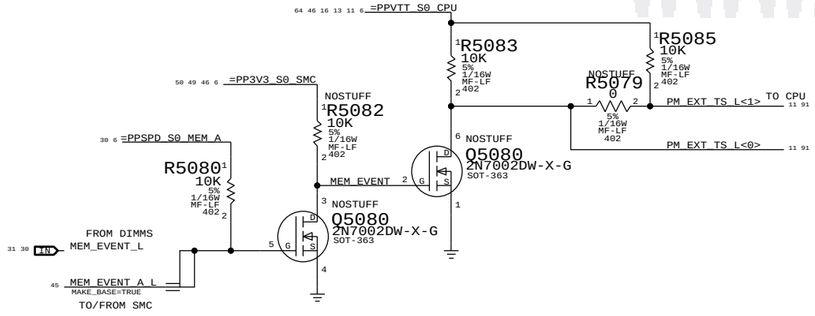


SMC AVREF Supply

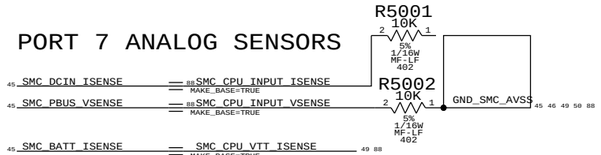


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

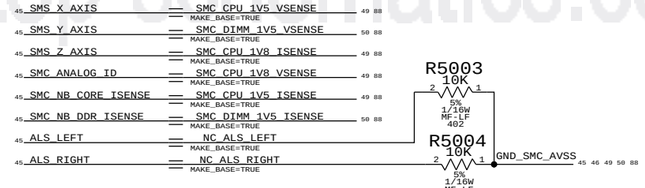
PM_EXTTS_L / MEM_EVENT LEVEL SHIFTING



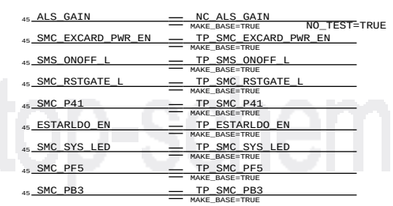
PORT 7 ANALOG SENSORS



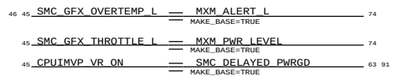
PORT D ANALOG SENSORS (INTERNAL PULLUPS)



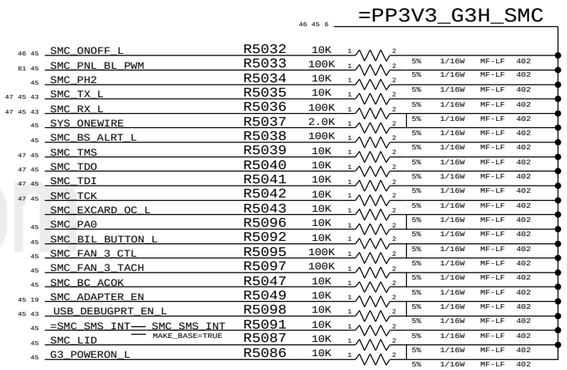
UNUSED TP/NC ALIASES



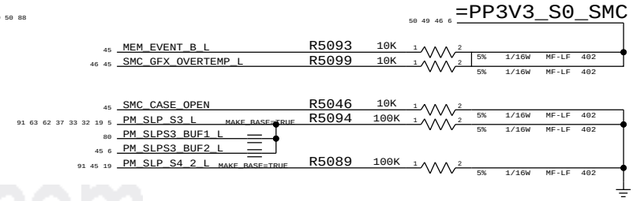
MISC. SIGNAL ALIASES



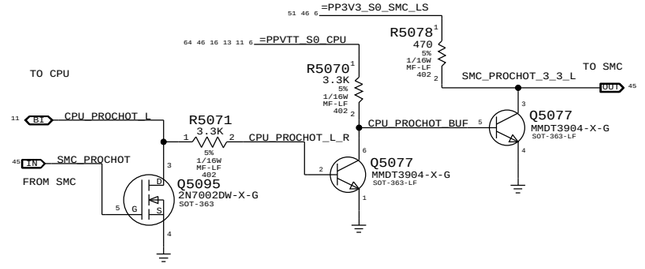
=PP3V3_G3H_SMC



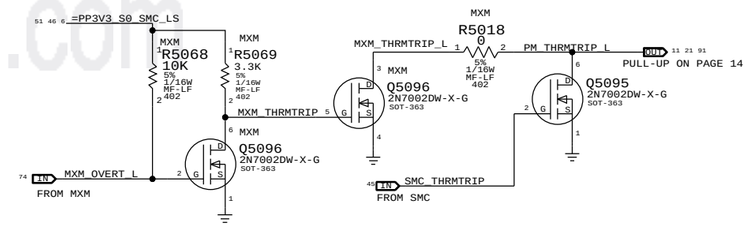
=PP3V3_S0_SMC



SMC PROCHOT 3.3V LEVEL SHIFTING



SMC & MXM THERMTRIP LEVEL SHIFTING



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: SMC Support

Apple Inc.

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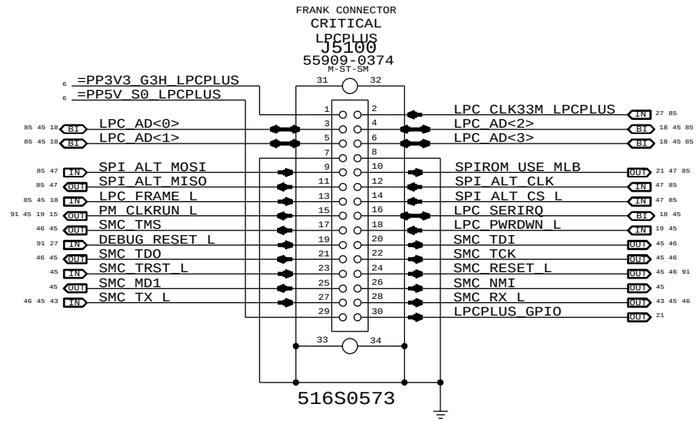
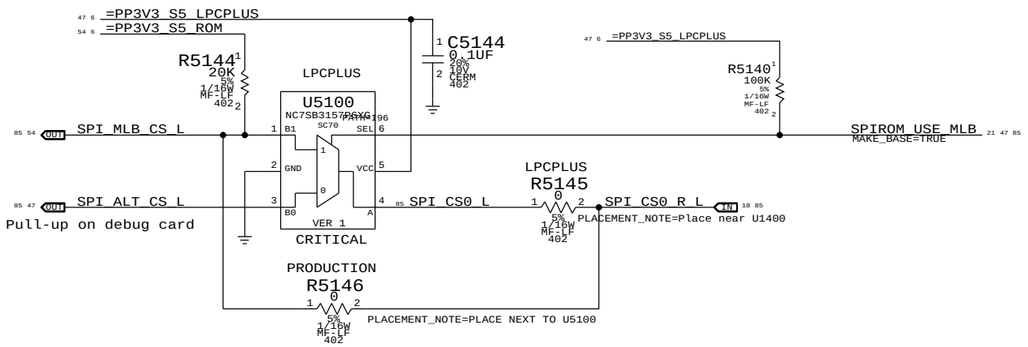
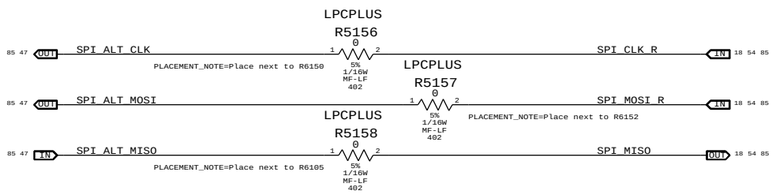
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
LPC+SPI Debug Connector

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PCH "SMBUS" CONNECTIONS

=PP3V3_S3_SMBUS

PCH
U1800
(MASTER)

SMBUS_PCH_CLK
MAKE_BASE=TRUE
SMBUS_PCH_DATA
MAKE_BASE=TRUE

NOSTUFF R5200 6.8K 5% 1/16W MF-LF 402
NOSTUFF R5201 6.8K 5% 1/16W MF-LF 402

MEMORY A VREF
U2900
(WRITE: 0X7C READ: 0X7D)
=I2C_VREFMRGN_A_SCL
=I2C_VREFMRGN_A_SDA

MEMORY B VREF
U2910
(WRITE: 0X5C READ: 0X5D)
=I2C_VREFMRGN_B_SCL
=I2C_VREFMRGN_B_SDA

PGOOD_P3V3_S0

NOSTUFF Q5200 SI2302ADSE3 SOT23-3-HF
R5211 0 5% 1/16W MF-LF 402

NOSTUFF Q5201 SI2302ADSE3 SOT23-3-HF
R5210 0 5% 1/16W MF-LF 402

MEMORY A DIMMS
J3100-A/B
(Write: 0xA0 Read: 0xA1)
(WRITE: 0XA2 READ: 0XA5)
=I2C_SODIMMA_SCL
=I2C_SODIMMA_SDA

MEMORY B DIMMS
J3200-A/B
(WRITE: 0XA4 READ: 0XA3)
(WRITE: 0XA6 READ: 0XA7)
=I2C_SODIMMB_SCL
=I2C_SODIMMB_SDA

=PP3V3_S0_SMBUS

R5208 3.3K 5% 1/16W MF-LF 402
R5209 3.3K 5% 1/16W MF-LF 402

MIKEY
U6806
(WRITE: 0X72 READ: 0X73)
=I2C_AUDIO_SCL
=I2C_AUDIO_SDA

XDP
J2500/J2550
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA

SMBUS_PCH_S0_CLK
MAKE_BASE=TRUE
SMBUS_PCH_S0_DATA
MAKE_BASE=TRUE

CK505
U2600
(WRITE: 0XD2 READ: 0XD3)
=SMBUS_CK505_SCL
=SMBUS_CK505_SDA

PCH "SML 0" CONNECTIONS

=PP3V3_S0_SMBUS

PCH
U1800
(MASTER)

SML_PCH_0_CLK
MAKE_BASE=TRUE
SML_PCH_0_DATA
MAKE_BASE=TRUE

R5202 8.2K 5% 1/16W MF-LF 402
R5203 8.2K 5% 1/16W MF-LF 402

SMC "B" SMBus Connections

=PP3V3_S0_SMBUS_SMC_B_S0

SMC
U4900
(MASTER)

SMB_B_S0_CLK
SMB_B_S0_DATA

SMBUS_SMC_B_S0_SCL
SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

R5260 2.2K 5% 1/16W MF-LF 402
R5261 2.2K 5% 1/16W MF-LF 402

REMOTE TEMPS
EMC1047-2, U5500, SEE TABLE
(WRITE: 0X90 READ: 0X91)
=SMB_REMOTE_TEMP_SCL
=SMB_REMOTE_TEMP_SDA

EMC1047-2 HEX DIODE SENSOR

DIODE	FUNCTION
1	ODD TEMP
2	LCD TEMP
3	AMBIENT TEMP
4	CPU HEATSINK
5	MXM HEATSINK

AC/DC PS TEMPS
EMC1403-[1,2]: ACDC THRU J600
(WRITE: 0X98 OR 0X9A, READ: 0X99 OR 0X9B)
3 SENSE POINTS - PRIMARY, SECONDARY, AMB
=SMB_ACDC_SCL
=SMB_ACDC_SDA

AC/DC PS POWER
INA219: ACDC THRU J600
(WRITE: 0X80, READ: 0X81))
OUTPUT VOLTAGE, CURRENT, POWER

SMC "A" SMBus Connections

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE

=PP3V3_S3_SMBUS_SMC_A_S3

SMC
U4900
(MASTER)

SMB_A_S3_CLK
SMB_A_S3_DATA

SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

R5270 4.7K 5% 1/16W MF-LF 402
R5271 4.7K 5% 1/16W MF-LF 402

ALS
(WRITE: 0X72 READ: 0X73)
TP_I2C_ALS_SCL
TP_I2C_ALS_SDA

POTENTIAL SMC SLAVE SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_BSA

THIS CONNECTION IS BROKEN THROUGH NOSTUFF RESISTORS ON PAGE 90

SMC
U4900
(MASTER)

SMB_BSA_CLK
SMB_BSA_DATA

SMBUS_SMC_BSA_SCL
SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

R5280 100K 5% 1/16W MF-LF 402
R5281 100K 5% 1/16W MF-LF 402

DISPLAY TCON
DP RX MASTER FOR MCCS
SMC SLAVE ADDRESS TBD
=SMB_DP_TCON_SCL
=SMB_DP_TCON_SDA

SMC "MANAGEMENT" SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_MGMT

SMC
U4900
(MASTER)

SMB_MGMT_CLK
SMB_MGMT_DATA

SMBUS_SMC_MGMT_SCL
SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

DP RX EQLZ CONTROL
U9200
(WRITE: 0X92 READ: 0X93)
=I2C_DP_EQLZ_SCL
=I2C_DP_EQLZ_SDA

DP TX EQLZ CONTROL
U9100
(WRITE: 0X9C READ: 0X9D)
=I2C_DP_DRV_SCL
=I2C_DP_DRV_SDA

PCH "SML 1" CONNECTIONS

=PP3V3_S0_SMBUS

PCH
U1800
(SLAVE)
(WRITE: 0X90 READ: 0X91)

SML_PCH_1_CLK
MAKE_BASE=TRUE
SML_PCH_1_DATA
MAKE_BASE=TRUE

NOSTUFF R5204 8.2K 5% 1/16W MF-LF 402
NOSTUFF R5205 8.2K 5% 1/16W MF-LF 402

R5206 0 5% 1/10W MF-LF 402
R5207 0 5% 1/10W MF-LF 402

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)

SMB_0_S0_CLK
SMB_0_S0_DATA

SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

MXM TEMP
GPU ON CARD - J8400
NV INSIDE (WRITE: 0X9E READ: 0X9F)
MXM CARD (WRITE: 0X98 READ: 0X99)
=SMB_MXM_THRM_SCL
=SMB_MXM_THRM_SDA

Also reserve 0x56 and 0x32 per spec

DIE TEMPS
EMC1402-2: U5535
(WRITE: 0X9A READ: 0X9B)
=SMB_CPU_THRM_SCL
=SMB_CPU_THRM_SDA
DIODE1: CPU

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
SMBus Connections

Apple Inc.

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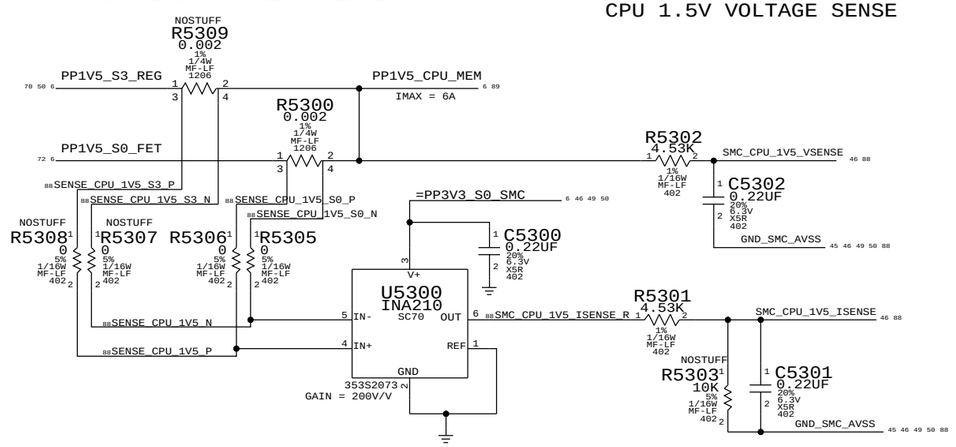
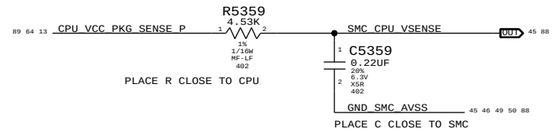
CPU 1.5V CURRENT SENSE

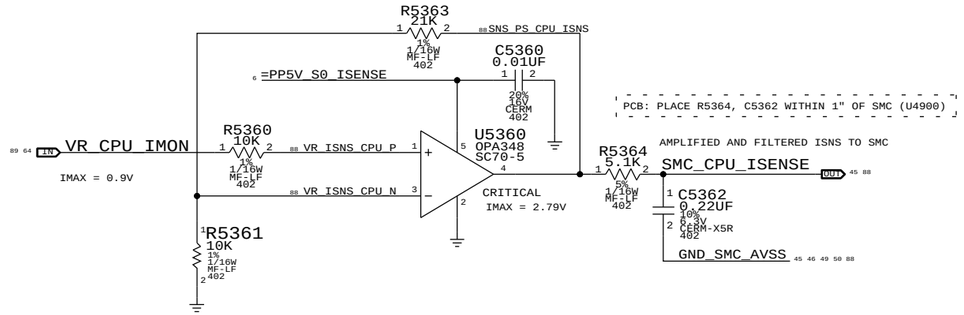


CPU 1.5V VOLTAGE SENSE

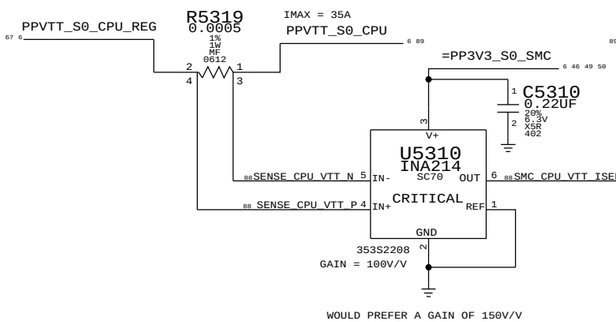
CPU Voltage Sense / Filter



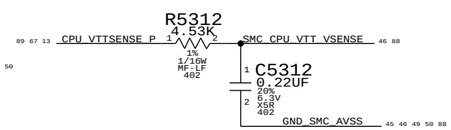
CPU CURRENT SENSE AMP & FILTER

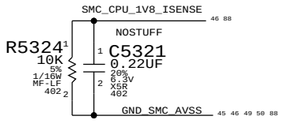


CPU VTT CURRENT SENSE



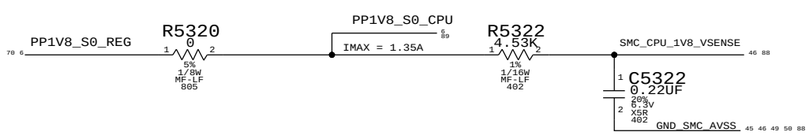
CPU VTT VOLTAGE SENSE





CPU 1.8V CURRENT SENSE

CPU 1.8V VOLTAGE SENSE



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

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CPU POWER SENSE

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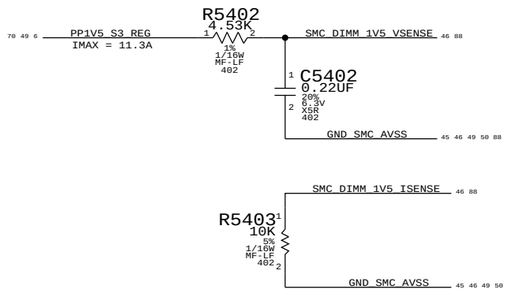
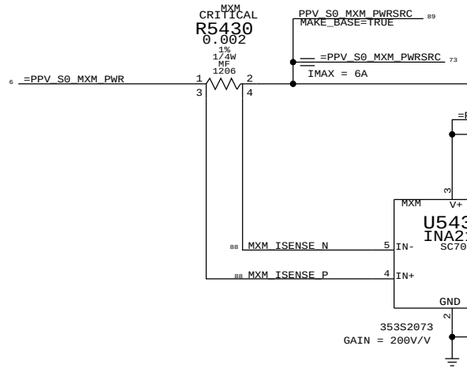
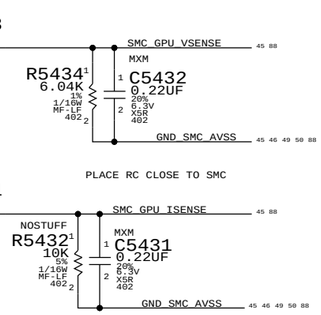
1.5V S3 VOLTAGE SENSE



MXM PWRSRC CURRENT SENSE



MXM PWRSRC VOLTAGE SENSE



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2016

PAGE TITLE
GRAPHICS / DIMM POWER SENSE

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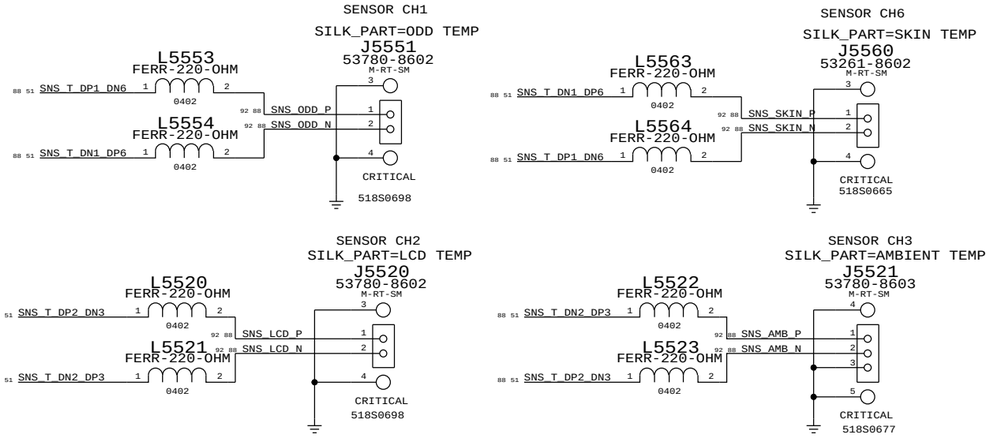
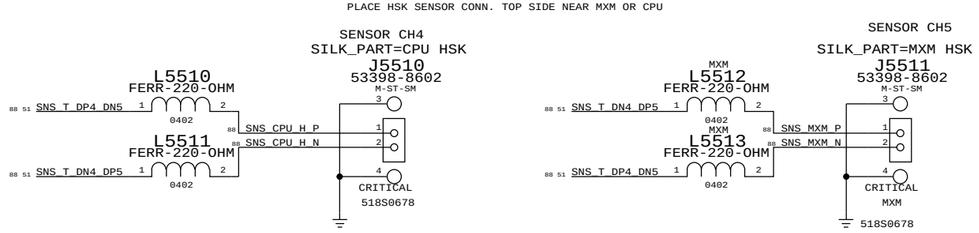
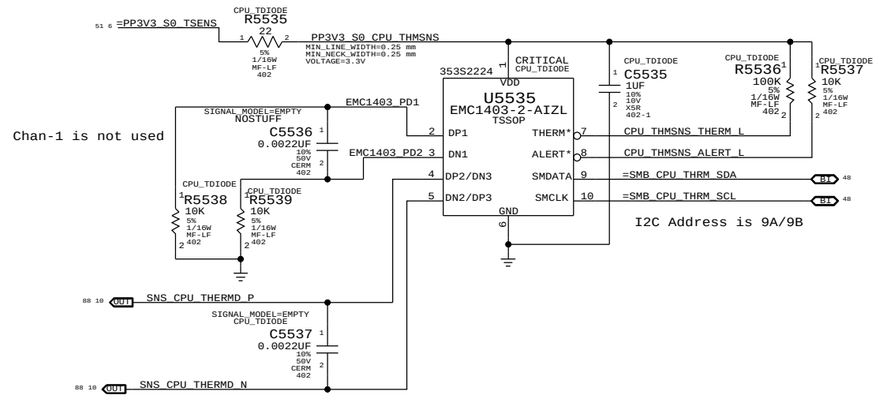
REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD



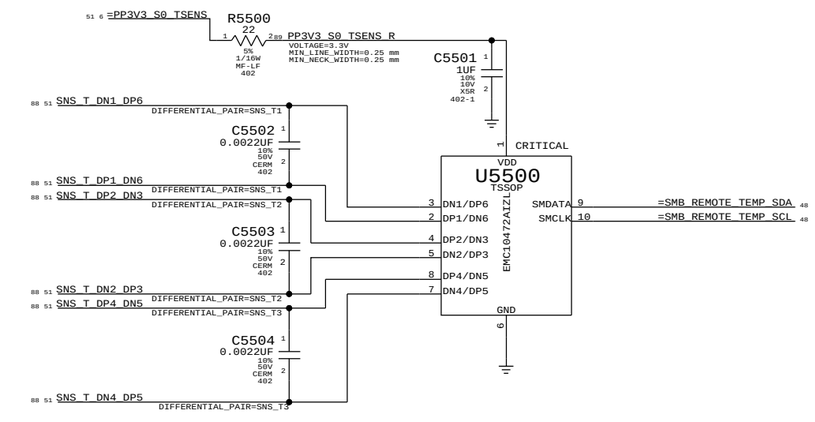
PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU



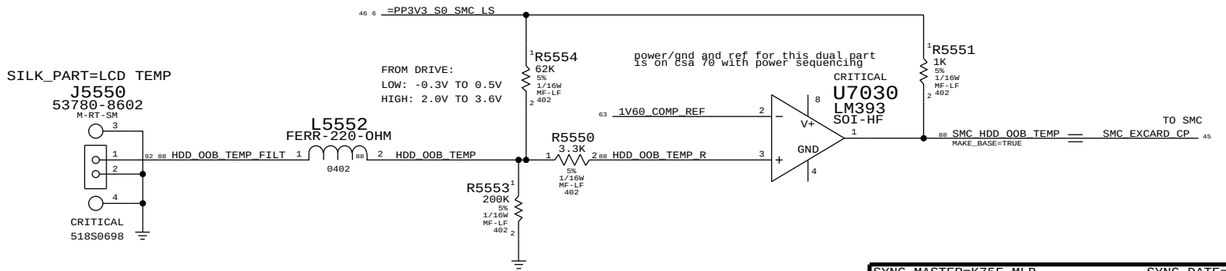
CPU T-DIODE THERMAL SENSOR



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: Thermal Sensors

Apple Inc.

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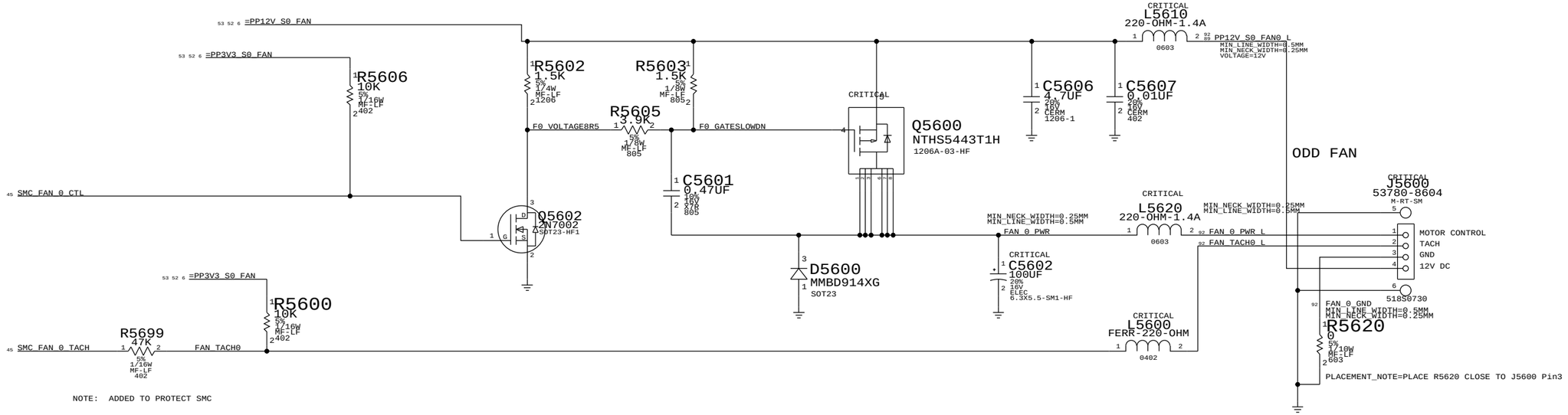
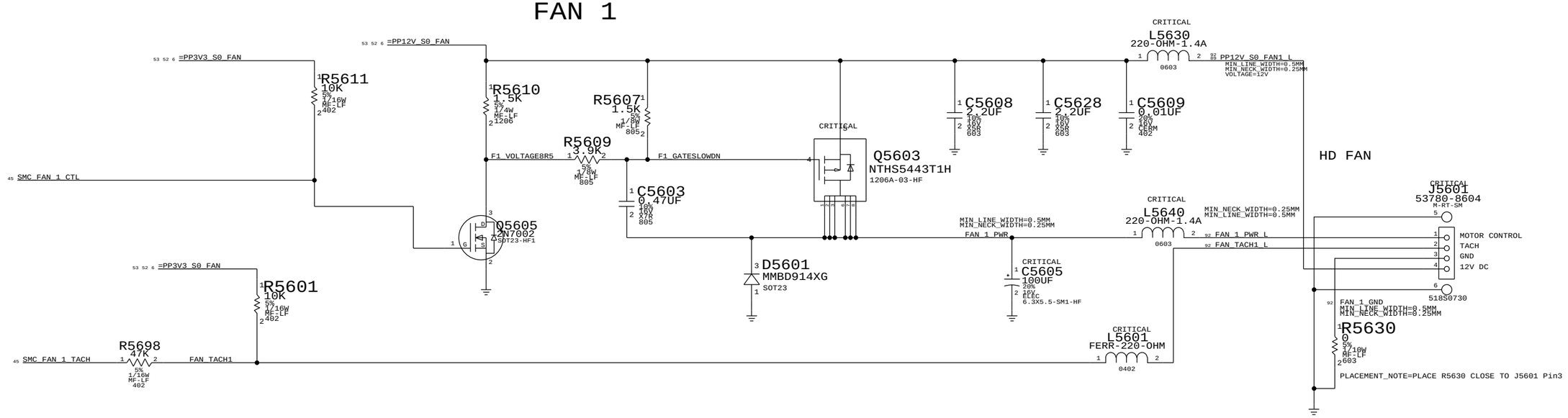
FAN 0



FAN 1



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

HD AND OD FAN

Apple Inc.

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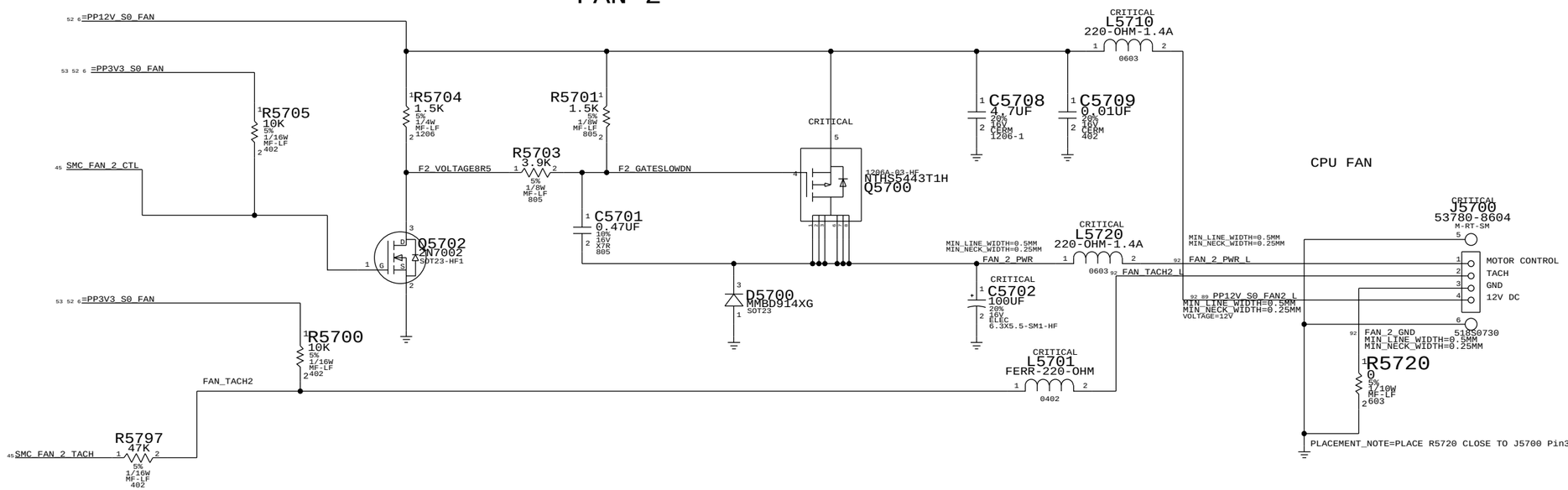
FAN 2



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: CPU FAN

Apple Inc.

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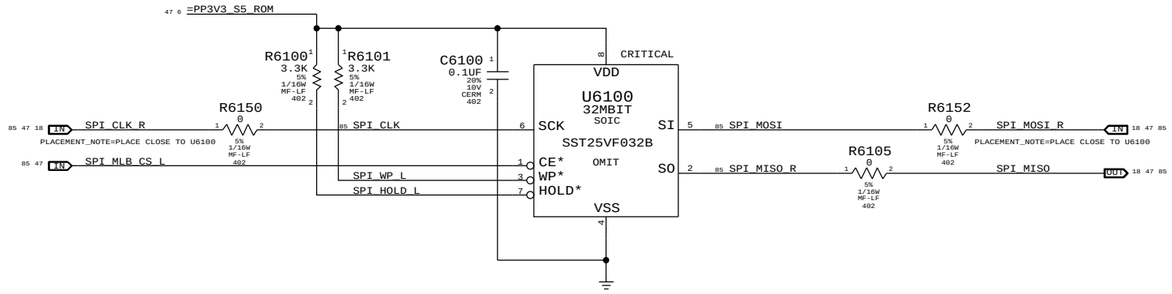

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

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SPI ROM

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AUDIO CODEC
APPLE P/N 353S2592

=PP1V5_S0_AUD_DIG

C6203 4.7UF 20% 4V X5R 402
C6258 0.47UF 10% 16V X5R 402
C6260 10UF 20% 16V POLY-TANT CASE-B2-SM
C6204 10UF 20% 6.3V X5R 603
C6205 10UF 20% 6.3V X5R 603
C6259 1UF 10% 16V X5R 402-1
C6264 0.47UF 10% 16V X5R 402
C6265 0.47UF 10% 16V X5R 402
C6261 0.47UF 10% 16V X5R 402
C6262 10UF 20% 16V POLY-TANT CASE-B2-SM
C6213 CRITICAL 10UF 20% 6.3V X5R 603

=PP5V_S0_AUDIO
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG VOLTAGE=4.5V MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM
GND_AUDIO_HP_AMP_L
GND_AUDIO_CODEC

R6255 2.67K 1% 1/16W MF-LF 402

K22 = NC
K23 LOW = S/PDIF IN, HIGH = DP SPDIF

U6201 CS4206ACNZC QFN

		VD	9	
		VA_REF	24	
		VA_HP	46	
		VA	25	
VBIAS_DAC	29	VBIAS_DAC		
CS4206_FP	44	VHP_FILT+		
CS4206_FN	41	VHP_FILT-		
AUD_MUX_CNTRL	2	GPIO0/DMIC_SDA1		
AUD_GPIO_1	12	GPIO1/DMIC_SDA2/SPDIF_OUT2		
AUD_GPIO_2	14	GPIO2		
AUD_GPIO_3	15	GPIO3		
AUD_SENSE_A	13	SENSE_A		
CS4206_FLYP	45	FLYP		
CS4206_FLYC	43	FLYC		
	42	FLYN		
CS4206_FLYN	3	VL_HD		
	1	VL_IF		
HDA_BIT_CLK	6	BITCLK		
HDA_SYNC	10	SYNC		
HDA_SDIN0	8	SDI		
HDA_SDOUT	5	SDO		
HDA_RST_L	11	RESET*		
AUD_SPDIF_IN_CODEC	47	SPDIF_IN		
AUD_SPDIF_CHIP	48	SPDIF_OUT		
		DGND THRM PAD AGND	7 49 26	
		CRITICAL HPOUT_L	38	AUD_HP_PORT_L
		HPOUT_R	40	AUD_HP_PORT_R
		HPREF	39	AUD_HP_PORT_REF
		LINEOUT_L1+	35	AUD_LO1_P_L
		LINEOUT_L1-	34	TP_AUD_LO1_N_L NC
		LINEOUT_R1+	36	AUD_LO1_P_R
		LINEOUT_R1-	37	TP_AUD_LO1_N_R NC
		LINEOUT_L2+	31	AUD_LO2_P_L
		LINEOUT_L2-	30	TP_AUD_LO2_N_L NC
		LINEOUT_R2+	32	AUD_LO2_P_R
		LINEOUT_R2-	33	TP_AUD_LO2_N_R NC
		MICBIAS	16	AUD_CODEC_MICBIAS
		VCOM	28	CS4206_VCOM
		LINEIN_L+	21	AUD_LI_P_L
		LINEIN_C-	22	AUD_LI_COM MAKE_BASE=TRUE
		LINEIN_R+	23	AUD_LI_P_R
		MICIN_L+	18	AUD_MIC_INP_L
		MICIN_L-	17	AUD_MIC_INN_L
		MICIN_R+	19	AUD_MIC_INP_R
		MICIN_R-	20	AUD_MIC_INN_R
		VREF+_ADC	27	CS4206_VREF_ADC NC
		DMIC_SCL	4	TP_AUD_DMIC_CLK NC

AUD_LI_N_L
AUD_LI_N_R

R6254 22 5% 1/16W MF-LF 402
R6257 22 5% 1/16W MF-LF 402
R6295 100K 1% 1/16W MF-LF 402
R6263 NOSTUFF 0 5% 1/16W MF-LF 402
R6267 NOSTUFF 100K 5% 1/16W MF-LF 402

C6211 CRITICAL 1UF 10% 20V TANT CASE-P3-HF
C6263 CRITICAL 10UF 20% 16V POLY-TANT CASE-B2-SM

XW6201 SM

GND_AUDIO_CODEC
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
GND_AUDIO_HP_AMP_L

BETTER
R6299 100K 5% 1/16W MF-LF 402
=PP3V3_S0_AUDIO
AUD_GPIO_1
EDUCATION
R6298 10K 5% 1/16W MF-LF 402

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

HP OUT ZOBEL NETWORK

MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
AUD_HP_PORT_L
AUD_HP_PORT_R
C6298 0.1UF 10% 16V X7R-CERM 402
C6297 0.1UF 10% 16V X7R-CERM 402
AUD_Z_R NC
AUD_Z_L NC
R6296 39 5% 1/16W MF-LF 402
R6297 39 5% 1/16W MF-LF 402
GND_AUDIO_HP_AMP_L

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=4.5V
L6201 FERR-220-OHM 0402
=PP5V_S0_AUDIO
R6201 2.21K 1% 1/16W MF-LF 402
=PP3V3_S0_AUDIO
VR6201 TPS71745 SON CRITICAL
IN
EN
4V5_REG_IN
4V5_REG_EN
OUT
NR/FB
GND
NC
4V5_NR
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=4.5V
PP4V5_AUDIO_ANALOG
C6201 1UF 10% 10V X5R 402-1
C6202 1UF 10% 10V X5R 402-1
C6266 0.1UF 10% 16V X7R-CERM 402
C6207 1UF 10% 10V X5R 402-1
GND_AUDIO_CODEC

SYNC_MASTER=K75F_MLB	SYNC_DATE=04/14/2010
PAGE TITLE	AUDIO: CODEC/REGULATOR
	Apple Inc.
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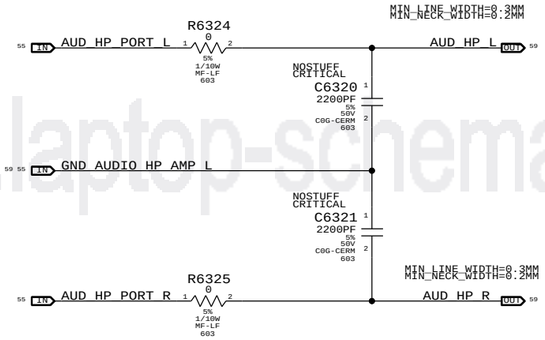
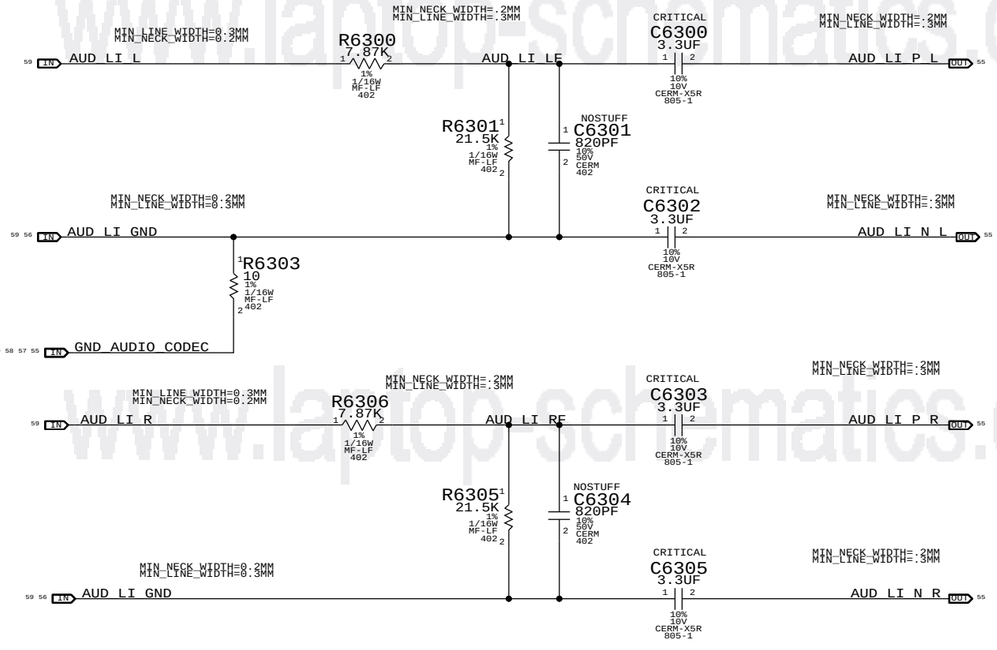
1ST ORDER DAC FILTER PLACEHOLDER



CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

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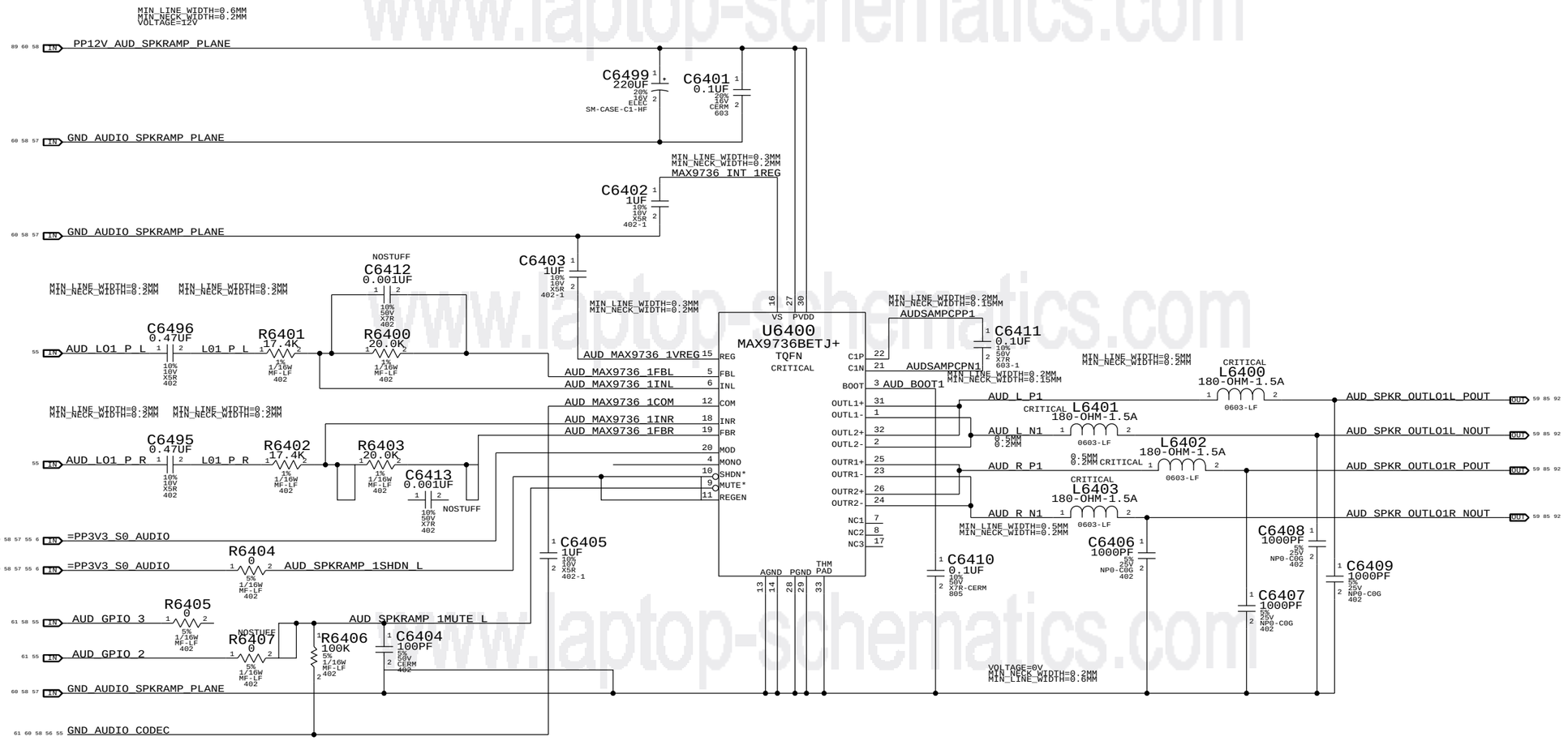
TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: AUDIO: Tweeter Amp 1

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D
REVISION: A.0.0
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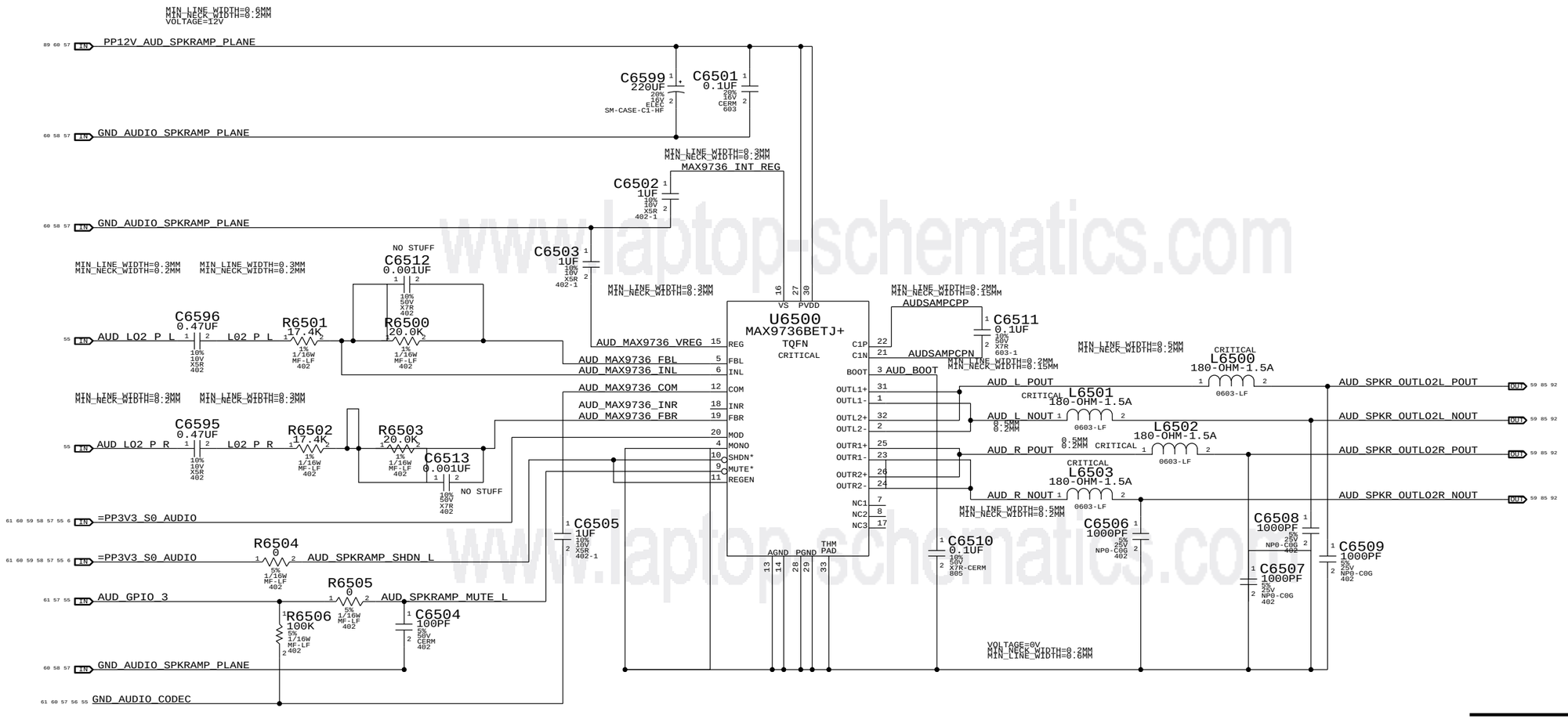
WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



SYNC_MASTER=K75F MLB SYNC_DATE=04/14/2010

PAGE TITLE
AUDIO: Woofer Amp

Apple Inc.

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INTERNAL MIC CON
APPLE P/N 518S0677

MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM

L6600
FERR-1000-OHM
0402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

L6601
FERR-1000-OHM
0402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

CRITICAL
J6601
53780-8603
M-RT-SM

86 60 OUT AUD_MIC1_IN_N

AUD_MIC_IN1_N_EMI

92 AUD_MIC_IN1_N_CONN

VOLTAGE=0V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

GND_AUDIO_MIC1_CONN

L6602
FERR-1000-OHM
0402

86 60 OUT AUD_MIC1_IN_P

AUD_MIC_IN1_P_EMI

L6603
FERR-1000-OHM
0402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

92 AUD_MIC_IN1_P_CONN

CRITICAL
DZ6600
6.8V-100PF
402

CRITICAL
DZ6601
6.8V-100PF
402

R6600
0
5%
1/10W
MF-LF
402

SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

PROPERTIES FOR ALL SPKR NETS

MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

CRITICAL
J6602
78048-0473
M-RT-SM

WOOFER (PRIMARY)

92 85 58 IN AUD_SPKR_OUTLO2R_POUT
92 85 58 IN AUD_SPKR_OUTLO2R_NOUT

TWEETER (SECONDARY)

85 57 92 IN AUD_SPKR_OUTLO1R_POUT
92 85 57 IN AUD_SPKR_OUTLO1R_NOUT

PROPERTIES FOR ALL SPKR NETS

MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

CRITICAL
J6603
78048-0573
M-RT-SM

WOOFER (PRIMARY)

92 85 58 IN AUD_SPKR_OUTLO2L_POUT
92 85 58 IN AUD_SPKR_OUTLO2L_NOUT

NO_TEST NC NC_J6702_3

TWEETER (SECONDARY)

92 85 57 IN AUD_SPKR_OUTLO1L_POUT
92 85 57 IN AUD_SPKR_OUTLO1L_NOUT

85 81 OUT AUD_SPDIF_IN

R6601
22
5%
1/10W
MF-LF
402

L6604
FERR-1000-OHM
0402

61 60 58 57 55 6 IN =PP3V3_S0_AUDIO

L6605
FERR-1000-OHM
0402

60 OUT AUD_LI_TIP_DET

MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM

R6610
0
5%
1/10W
MF-LF
603

56 OUT AUD_LI_GND

MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM

L6607
FERR-1000-OHM
0402

56 OUT AUD_LI_R

MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM

L6608
FERR-1000-OHM
0402

56 OUT AUD_LI_L

MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=0V

L6609
FERR-1000-OHM
0402

61 OUT HS_MIC_LO

MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.1MM

L6606
FERR-1000-OHM
0402

61 OUT HS_MIC_HI

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

XW6617
SM

55 OUT AUD_HP_PORT_REF

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

R6617
0
5%
1/10W
MF-LF
603

56 55 OUT GND_AUDIO_HP_AMP_L

MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM

L6616
220-OHM-0.7A-0.28-OHM
0402

56 IN AUD_HP_L

MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

L6618
220-OHM-0.7A-0.28-OHM
0402

56 IN AUD_HP_R

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

L6614
FERR-1000-OHM
0402

60 OUT AUD_HP_TYPE

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

L6615
FERR-1000-OHM
0402

60 OUT AUD_IP_PERPH_DET

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

L6612
FERR-1000-OHM
0402

60 OUT AUD_HP_TIP_DET

L6613
FERR-1000-OHM
0402

85 55 IN AUD_SPDIF_OUT

REMOTE I/O CONNECTOR
APPLE P/N 518S0723

CRITICAL
J6600
20143-020E-20F
F-RT-SM

1	AUD_SPDIFIN_JACK
2	
3	89 PP3V3_AUDIO_SPDIF_JACK
4	AUD_LI_DET_JACK
5	AUD_LI_GND_JACK
6	AUD_LI_R_JACK
7	AUD_LI_GND_JACK
8	AUD_LI_L_JACK
9	HS_MIC_LO_JACK
10	HS_MIC_HI_JACK
11	AUD_HP_GND_JACK
12	AUD_HP_L_JACK
13	AUD_HP_GND_JACK
14	AUD_HP_R_JACK
15	AUD_HP_TYPEDET_JACK
16	AUD_IP_PERPH_JACK
17	AUD_HP_TIPDET_JACK
18	PP3V3_AUDIO_SPDIF_JACK
19	AUD_SPDIF_OUT_JACK
20	
21	
22	
23	
24	

MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM VOLTAGE=3.3V

MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM

MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM

CRITICAL DZ6603 6.8V-100PF 402
CRITICAL DZ6604 6.8V-100PF 402
CRITICAL DZ6605 6.8V-100PF 402
CRITICAL DZ6606 6.8V-100PF 402
CRITICAL DZ6607 6.8V-100PF 402
CRITICAL DZ6608 6.8V-100PF 402
CRITICAL DZ6609 6.8V-100PF 402
CRITICAL DZ6610 6.8V-100PF 402
CRITICAL DZ6611 6.8V-100PF 402
CRITICAL DZ6612 6.8V-100PF 402
CRITICAL DZ6613 6.8V-100PF 402
CRITICAL DZ6614 6.8V-100PF 402
CRITICAL DZ6615 6.8V-100PF 402

C6600 1UF 10% 10V X5R 402-1

C6601 0.47UF 10% 10V X5R 402

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Audio: MLB to I/O Conn.

Apple Inc.

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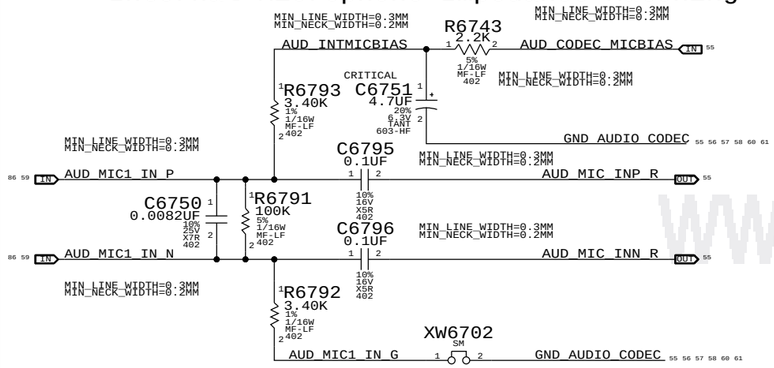
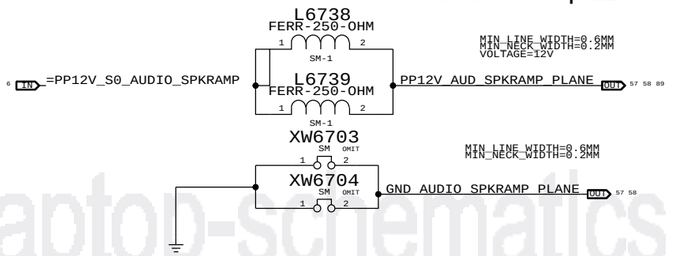
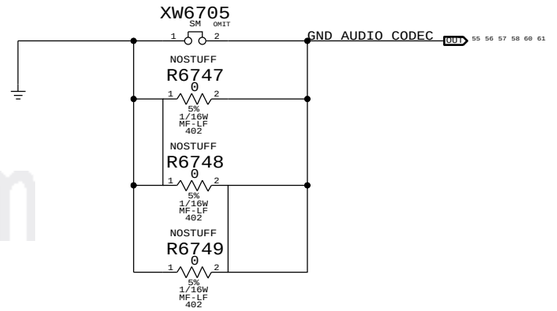
Internal Microphone Impedance Matching



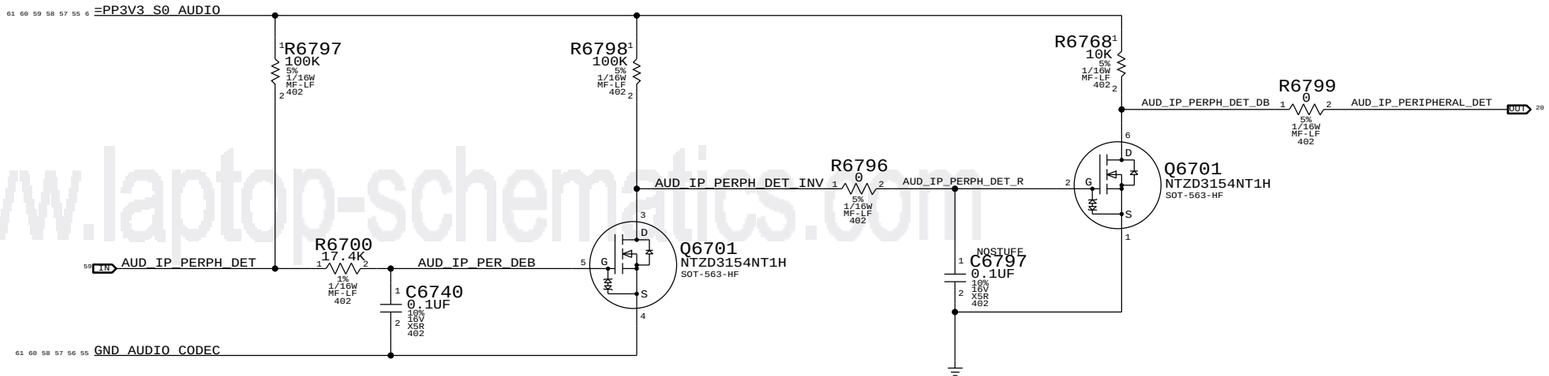
Place Across Ground Split



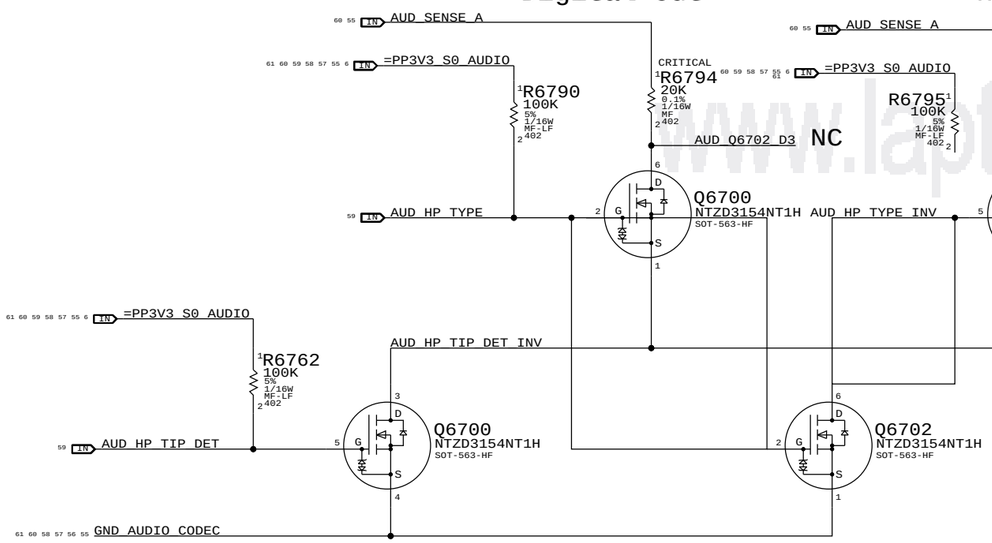
Audio Ground Returns



IPHS HS Detect Debounce CKT

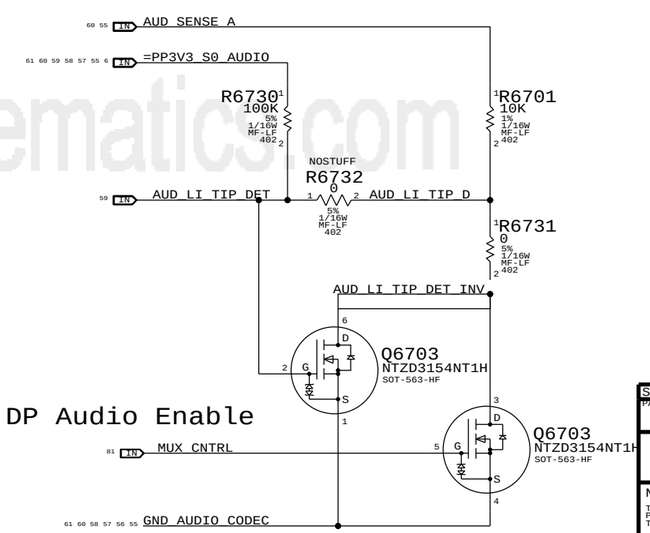


Digital Out



Headphone Out

LI Insert Detect



DP Audio Enable

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

AUDIO: Detects/Grounding

Apple Inc.

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FUNCTION	PIN
PRIMARY	0X0B
SECONDARY	0X0A
HEADPHONES	0X09
LINE INPUT	0X0C
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)
SPDIF OUT	0X10
SPDIF IN	0X0F
MIKEY	N/A

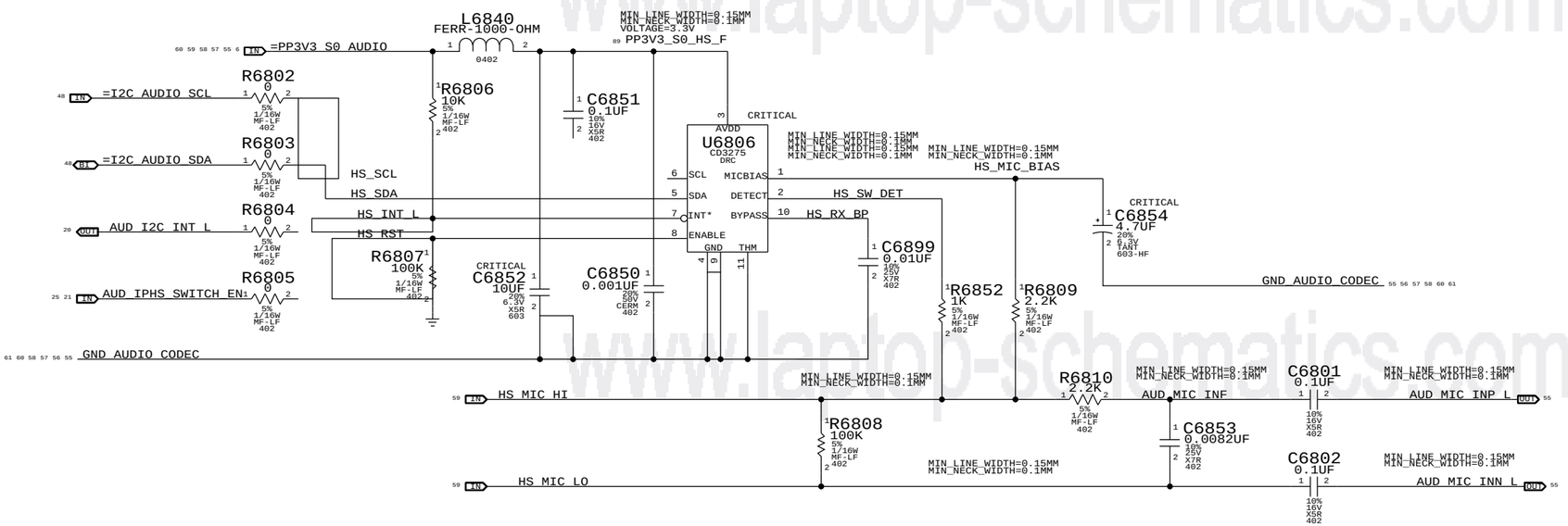
CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
0X04	0X04	GPIO 3	N/A
0X03	0X03	GPIO 3	N/A
0X02	0X02	N/A	0X09 (A)
0X05	0X05	N/A	LINE IN
0X06	0X06	MICBIAS 80%	N/A
0X06	0X06	MIKEY	MIKEY
0X08	N/A	N/A	0X0C (B)
0X07	N/A	N/A	N/A
N/A	N/A	MCP GPIO_38	MCP GPIO_5

=PP5V_S0_AUDIO

C6857 1UF 10V X5R 402-1

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256



AUD_GPIO_2

NOSTUFF D6800 1N4148WS-X-G SOD-323-HF

AUD_GPIO_3

FLP = 8.82 KHZ
FHP = 80 HZ

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: AUDIO: Mikey

Apple Inc.

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SLP_S4 ENABLES

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

R6901 0 5% 1/16W MF-LF 402
91 45 IN PM_RSMRST_L 1 2 PM_RSMRST_PCH_L OUT 19 91

MEMVTT_EN SEQUENCE
72 63 62 6 5 =PP3V3_S0_PWRCTL
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
R6953 0 5% 1/16W MF-LF 402
DDRVTT_EN 32 62 70 91
NOSTUFF C6951 100PF 5% 50V CERM 402
VTT_REG_PGOOD_R1
VTT_REG_PGOOD_R2
Q6911 MMDT3904-X-G SOT-363-LF
NOSTUFF C6953 0.1UF 10% 16V X5R 402
R6950 100K 5% 1/16W MF-LF 402
67 63 62 11 91 CPUVTT_REG_PGOOD
CPUVTT_RP_R
Q6911 MMDT3904-X-G SOT-363-LF
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

63 62 6 5 =PP3V3_S5_PWRCTL
C6910 0.1UF 20% 10V CERM 402
91 19 PM_SLP_S4_1_L
74LVC08 TSSOP-HF
U6900 08
S4_ENABLES
R6911 33 5% 1/16W MF-LF 402
R6912 33 5% 1/16W MF-LF 402
R6914 33 5% 1/16W MF-LF 402
P3V3S3_EN 72 91 Enable FET
P5VS3_EN 69 91 ENABLE REGULATOR
P12V_S3_EN 72 91 Enable FET
NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6923 0.47UF 10% 6.3V CERM-X5R 402

63 62 6 5 =PP3V3_S5_PWRCTL
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC
Q6910 2N7002DW-X-G SOT-363
11 CPU_SKTOCC_L
NOSTUFF R6917 0 5% 1/16W MF-LF 402
PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

6 =PP5V_S3_PWRCTL
R6910 100K 5% 1/16W MF-LF 402
69 P5VS3_REG_PGOOD MAKE_BASE=TRUE
PM_EN_USB_PWR 43
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402
=DDRREG_EN 70

SLP_M ENABLES

THIS SLP_M CIRCUIT IS A BACKUP IN CASE
VCC_ME IS REQUIRED IN ANY STATE
OTHER THAN S0. DELETE AFTER PROTO1

NOSTUFF R6920 33 5% 1/16W MF-LF 402
Enable FET P3V3ME_EN 72 91
PLACE SERIES R'S NEAR SOURCE

R6922 1K 5% 1/16W MF-LF 402
91 19 5 PM_SLP_M_L
P1V05_ME_SM_EN 72 91 Enable FET
R6927 0 5% 1/16W MF-LF 402
72 63 62 6 5 =PP3V3_S0_PWRCTL
=PP3V3_S5_PWRCTL
C6925 1UF 10% 6.3V CERM 402
P1V05_SM_DIS_L
R6925 10K 5% 1/16W MF-LF 402
62 PM_SLP_S3_BUF_L
PM_SLP_S3_B_R
74LVC08 TSSOP-HF U6900 08
PCHCORE_PGOOD_R
P1V05_ME_SM_DIS
Q6910 2N7002DW-X-G SOT-363
R6926 10K 5% 1/16W MF-LF 402
68 63 62 6 91 PCHCORE_REG_PGOOD
C6926 1UF 10% 6.3V CERM 402

SLP_S3 ENABLES

63 62 6 5 =PP3V3_S5_PWRCTL
91 63 46 37 33 32 19 5 PM_SLP_S3_L
74LVC08 TSSOP-HF U6900 08
(PM_SLP_S3_L_BUF)
MAKE_BASE=TRUE
63 PGOOD_P12V_S0
R6944 10K 1% 1/16W MF-LF 402
NOSTUFF R6941 10K 5% 1/16W MF-LF 402
R6946 33 5% 1/16W MF-LF 402
P3V3S0_EN Enable FET OUT 72 91
R6947 33 5% 1/16W MF-LF 402
P5VS0_EN Enable FET OUT 72 91
OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)
PM_SLP_S3_BUF_L 62
R6948 0 5% 1/16W MF-LF 402
91 70 5 PM_PGOOD_DDRREG_S3
switch to alias after proto1
Enable FET P1V5_S0_EN 72 91
DDRVTT_EN 32 62 70 91 Enable regulator
NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

72 63 62 6 5 =PP3V3_S0_PWRCTL
R6942 10K 5% 1/16W MF-LF 402
Enable regulator PCHCORE_REG_EN
PCHCORE VREG
68 91 91 68 63 62 5 PCHCORE_REG_PGOOD MAKE_BASE=TRUE
ENABLE FET P1V05_ME_S0_EN 72
91 72 PGOOD_P5V_S0 MAKE_BASE=TRUE
C6942 1UF 10% 6.3V CERM 402
R6949 0 5% 1/16W MF-LF 402
Enable regulator CPUVTT_REG_EN
CPUVTT VREG
67 91 91 67 63 62 11 CPUVTT_REG_PGOOD MAKE_BASE=TRUE
Enable regulator PM_EN_PVCORE_CPU 64
TO ENABLE OF CPU VREG
switch to alias after proto1

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2016
PAGE TITLE
POWER SEQUENCING ENABLES
Apple Inc.
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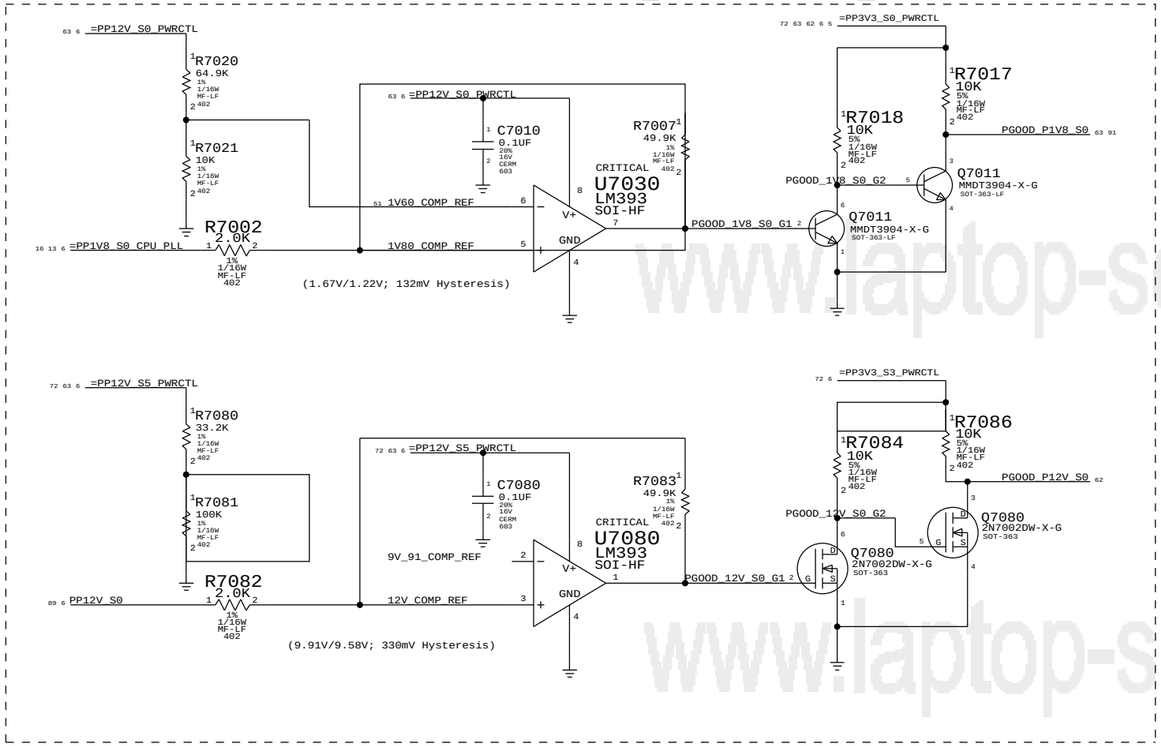
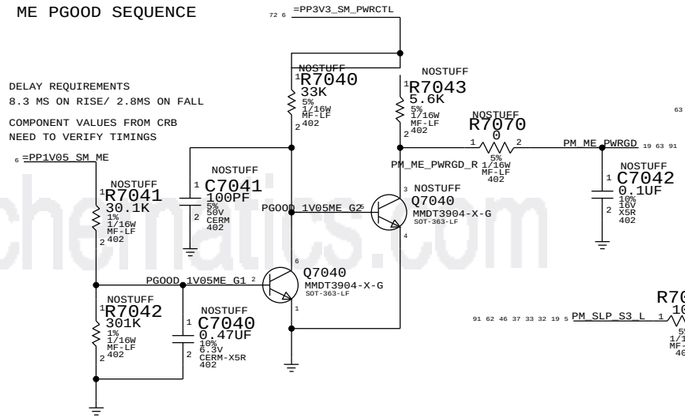
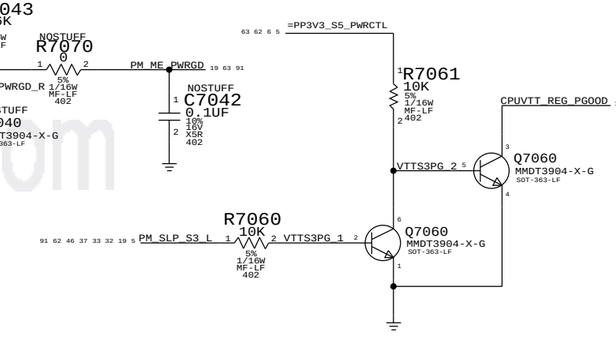
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0



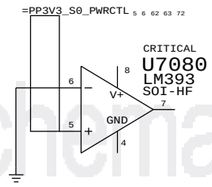
S0 RAILS PGOOD

ME PGOOD SEQUENCE

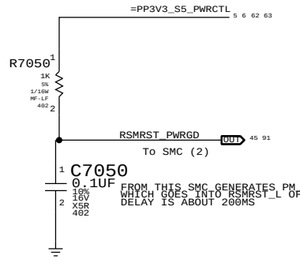




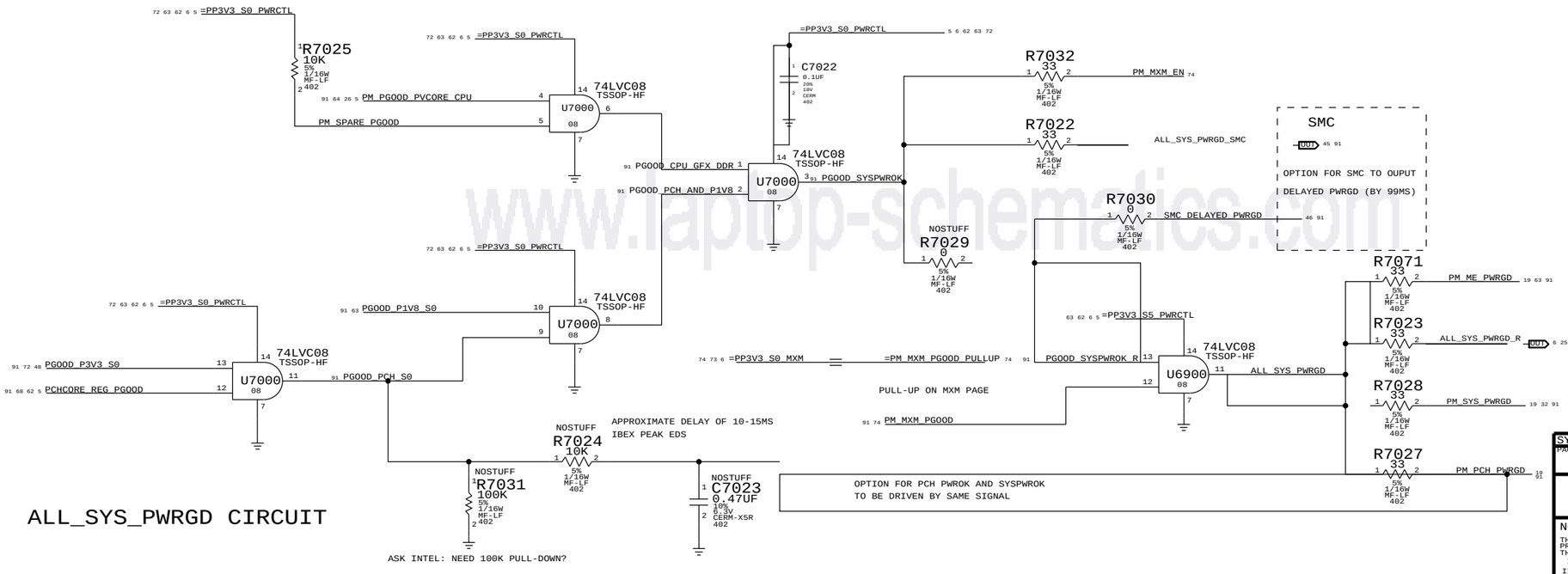
DISABLE CPUVTT_REG_PGOOD WHEN SLP_S3_L = 0 (PER PIKETON PDG)



SPARE



ALL_SYS_PWRGD CIRCUIT



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: POWER SEQUENCING PGOOD

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

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CPU CORE REG 1.1V/110A O/P= PPVCORE_S0_CPU_REG

CPU VCORE
VOUT = VCORE
PEAK = 110A
AVG = 90A

=PP5V_S0_VRD
PPVCORE_S0_CPU_REG
CPU_VCC_PKG_SENSE_P
CPU_VCC_PKG_SENSE_N
PP5V_S0_CPU_VCORE_VCC
=PP3V3_S0_VRD
=PPVTT_S0_CPU
PM_EN_PVCORE_CPU
PM_PGOOD_PVCORE_CPU
VR_CPU_IOUT
CPU_PSI_L
CPU_VID<7..0>
=PP12V_S0_VRD
IMAX = 10.5A
PP12V_S0_CPU_FLTRD
NET_PHYSICAL_TYPE=POWER
VOLTAGE=12V
PP5V_S0_CPU_VCORE_VCC
MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=5V
LOCAL 5V
AGND_CPU
VR_CPU_FB_R
VR_CPU_COMP_R
VR_CPU_COMP_RC
VR_CPU_VSEN
SIGNAL_MODEL=EMPTY
1.25 mOhm loadline
VR_CPU_VSNS_R_P
VR_CPU_VSNS_R_N
VR_CPU_RGND
VR_VDF_R1
VR_VDF_R2
VR_CPU_COMP
VR_CPU_FB
VR_CPU_VDIFF
VR_CPU_TCOMP
VR_CPU_OFS
VR_CPU_FS
VR_CPU_SS
VR_CPU_DAC
VR_CPU_REF
VR_CPU_TM
VR_CPU_EN_VTT
VR_CPU_IMON
VR_CPU_FAN
VR_CPU_VRDHOT
VR_CPU_EN_PWR
VR_CPU_IOUT_PD
VR_HOT goes HIGH when VTM/VCC < 28% and LOW when VTM/VCC > 33%.
LAYOUT: PLACE RT7101 NEAR HOT SPOT.
U7100 ISL6334 QFN
CRITICAL
SYM_VER_2
VCC
THRM_PAD
PWM1 PWM2 PWM3 PWM4
ISEN1+ ISEN1- ISEN2+ ISEN2- ISEN3+ ISEN3- ISEN4+ ISEN4-
COMP FB VDIFF VSEN RGND TCOMP OFS FS SS DAC REF TM EN_VTT RDY VID0 VID1 VID2 VID3 VID4 VID5 VID6 VID7 PSI* IMON VR_FAN VR_HOT EN_PWR
VR_CPU_PWM1 VR_CPU_PWM2 VR_CPU_PWM3 VR_CPU_PWM4
VR_CPU_ISNS1_R_P VR_CPU_ISNS1_R_N VR_CPU_ISNS2_R_P VR_CPU_ISNS2_R_N VR_CPU_ISNS3_R_P VR_CPU_ISNS3_R_N VR_CPU_ISNS4_R_P VR_CPU_ISNS4_R_N
VR_CPU_ISNS1_RR_2 VR_CPU_ISNS2_RR_2 VR_CPU_ISNS3_RR_2 VR_CPU_ISNS4_RR_2
VR_CPU_ISNS1_P VR_CPU_ISNS1_N VR_CPU_ISNS2_P VR_CPU_ISNS2_N VR_CPU_ISNS3_P VR_CPU_ISNS3_N VR_CPU_ISNS4_P VR_CPU_ISNS4_N
OMIT XW7120 XW7130 XW7101
NOSTUFF
D7171 NSR0140P2T5G SOD-923-HF
CRITICAL L7100 0.36UH-45A-0.76MOHM MSQ1211R36LF-TH
152-0104
CPU CORE INPUT Filtering

SYNC_MASTER=K75F_MLB	SYNC_DATE=04/14/2010
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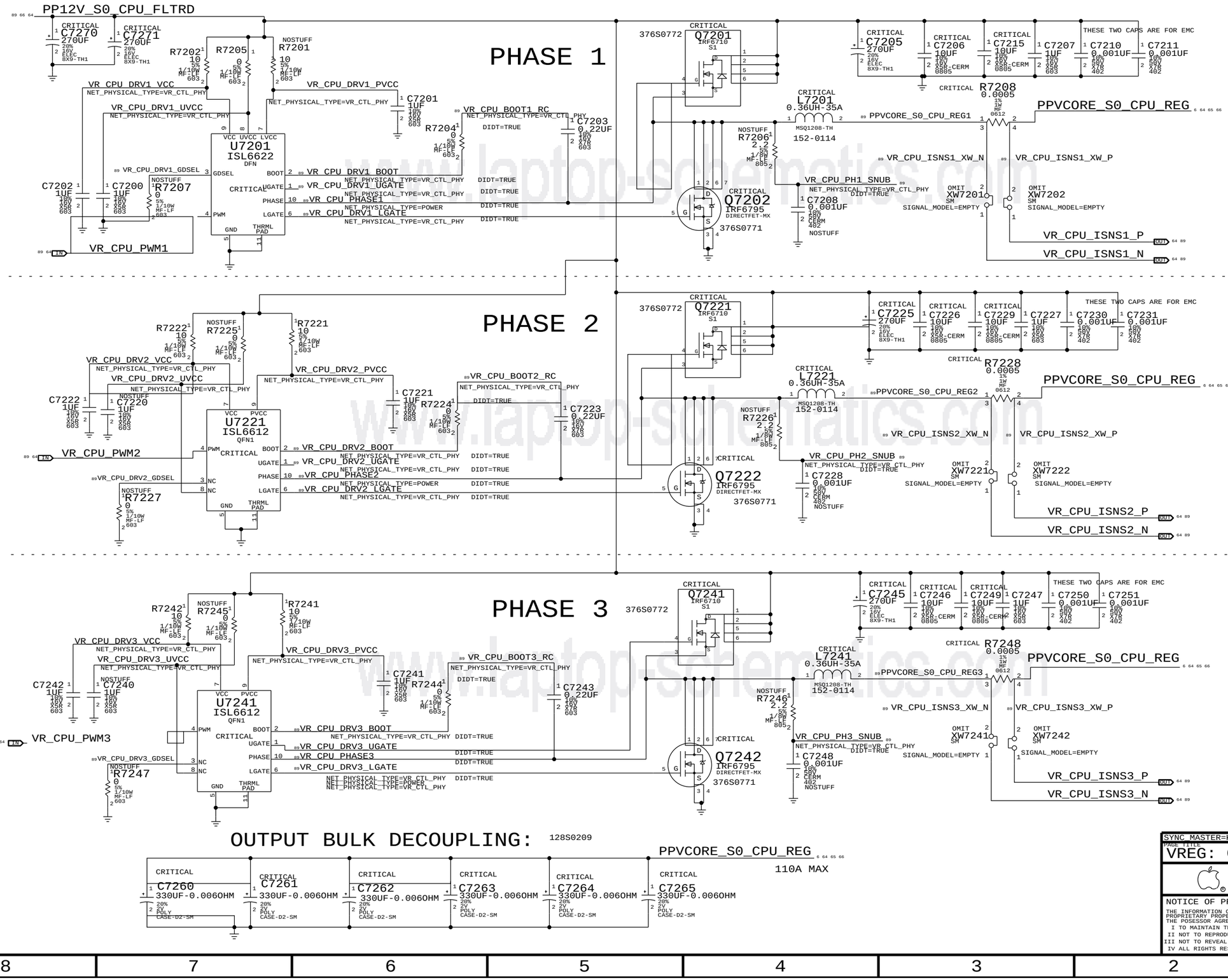
PHASE 1
PP12V_S0_CPU_FLTRD
U7201
ISL6622
VR_CPU_DRV1_VCC
VR_CPU_DRV1_UVCC
VR_CPU_DRV1_PVCC
VR_CPU_DRV1_GDSEL
VR_CPU_DRV1_BOOT
VR_CPU_DRV1_UGATE
VR_CPU_PHASE1
VR_CPU_DRV1_LGATE
VR_CPU_BOOT1_RC
VR_CPU_PWM1
Q7201
IRF6710
Q7202
IRF6795
376S0772
376S0771
L7201
0.36UH-35A
PPVCORE_S0_CPU_REG1
VR_CPU_PH1_SNUB
VR_CPU_ISNS1_XW_N
VR_CPU_ISNS1_XW_P
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N
PHASE 2
U7221
ISL6612
VR_CPU_DRV2_VCC
VR_CPU_DRV2_UVCC
VR_CPU_DRV2_PVCC
VR_CPU_DRV2_GDSEL
VR_CPU_DRV2_BOOT
VR_CPU_DRV2_UGATE
VR_CPU_PHASE2
VR_CPU_DRV2_LGATE
VR_CPU_BOOT2_RC
VR_CPU_PWM2
Q7221
Q7222
L7221
PPVCORE_S0_CPU_REG2
VR_CPU_PH2_SNUB
VR_CPU_ISNS2_XW_N
VR_CPU_ISNS2_XW_P
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N
PHASE 3
U7241
ISL6612
VR_CPU_DRV3_VCC
VR_CPU_DRV3_UVCC
VR_CPU_DRV3_PVCC
VR_CPU_DRV3_GDSEL
VR_CPU_DRV3_BOOT
VR_CPU_DRV3_UGATE
VR_CPU_PHASE3
VR_CPU_DRV3_LGATE
VR_CPU_BOOT3_RC
VR_CPU_PWM3
Q7241
Q7242
L7241
PPVCORE_S0_CPU_REG3
VR_CPU_PH3_SNUB
VR_CPU_ISNS3_XW_N
VR_CPU_ISNS3_XW_P
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N
OUTPUT BULK DECOUPLING:
128S0209
PPVCORE_S0_CPU_REG
110A MAX
C7260
C7261
C7262
C7263
C7264
C7265
330UF-0.006OHM
THESE TWO CAPS ARE FOR EMC
PPVCORE_S0_CPU_REG
R7208
R7228
R7248
0.0005
SYNC_MASTER=K75F_MLB
SYNC_DATE=04/14/2010
PAGE TITLE
VREG: CPU CORE - PHASES 1-3
Apple Inc.
DRAWING NUMBER
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PHASE 4

PP12V_S0_CPU_FLTRD

R7311 10 5% 1/10W MF-LF 603
R7312 NOSTUFF 0 5% 1/10W MF-LF 603
R7313 10 5% 1/10W MF-LF 603

VR_CPU_DRV4_VCC (NET_PHYSICAL_TYPE=VR_CTL_PHY)
VR_CPU_DRV4_UVCC (NET_PHYSICAL_TYPE=VR_CTL_PHY)
VR_CPU_DRV4_PVCC (NET_PHYSICAL_TYPE=VR_CTL_PHY)

C7312 1UF 10% 16V X5R 603
C7310 NOSTUFF 1UF 10% 16V X5R 603
C7311 1UF 10% 16V X5R 603

U7301 ISL6612 QFN1
VCC PVCC PWM BOOT UGATE PHASE NC NC LGATE GND THRML PAD

VR_CPU_PWM4
VR_CPU_DRV4_GDSEL
R7310 NOSTUFF 0 5% 1/10W MF-LF 603

VR_CPU_DRV4_BOOT (NET_PHYSICAL_TYPE=VR_CTL_PHY, DIDT=TRUE)
VR_CPU_DRV4_UGATE (NET_PHYSICAL_TYPE=VR_CTL_PHY, DIDT=TRUE)
VR_CPU_PHASE4 (NET_PHYSICAL_TYPE=POWER, DIDT=TRUE)
VR_CPU_DRV4_LGATE (NET_PHYSICAL_TYPE=VR_CTL_PHY, DIDT=TRUE)

VR_CPU_BOOT4_RC (NET_PHYSICAL_TYPE=VR_CTL_PHY, DIDT=TRUE)
R7303 0 5% 1/10W MF-LF 603
C7303 0.22UF 10% 16V X5R 603

376S0772
CRITICAL Q7301 IRF6710 S1

CRITICAL L7301 0.36UH-35A MSQ120B-TH 152-0114

CRITICAL Q7302 IRF6795 DIRECTFET-MX
376S0771

NOSTUFF R7302 2.2 5% 1/8W MF-LF 805

VR_CPU_PH4_SNUB (NET_PHYSICAL_TYPE=VR_CTL_PHY, DIDT=TRUE)
C7302 0.001UF 10% 50V CERM 402 NOSTUFF

THESE TWO CAPS ARE FOR EMC

CRITICAL C7304 270UF 20% 2V TCEC 6X9-TH1
CRITICAL C7305 10UF 10% 16V X5R CERM 0805
CRITICAL C7306 10UF 10% 16V X5R CERM 0805
C7307 1UF 10% 16V X5R 603
C7308 0.001UF 10% 50V X7R 402
C7309 0.001UF 10% 50V X7R 402

CRITICAL R7301 0.0005 1% 1W MF 0612

PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU_REG4

VR_CPU_ISNS4_XW_N
VR_CPU_ISNS4_XW_P

XW7301 OMIT SM SIGNAL_MODEL=EMPTY
XW7302 OMIT SM SIGNAL_MODEL=EMPTY

VR_CPU_ISNS4_P
VR_CPU_ISNS4_N

PPVCORE_S0_CPU_REG

C7330 0.1UF 20% 10V CERM 402
C7331 0.1UF 20% 10V CERM 402
C7332 0.1UF 20% 10V CERM 402
C7333 0.1UF 20% 10V CERM 402
C7334 0.1UF 20% 10V CERM 402
C7335 0.1UF 20% 10V CERM 402
C7336 0.1UF 20% 10V CERM 402
C7337 0.1UF 20% 10V CERM 402
C7338 0.1UF 20% 10V CERM 402
C7339 0.1UF 20% 10V CERM 402

C7340 1UF 10% 16V X5R 603
C7341 1UF 10% 16V X5R 603
C7342 1UF 10% 16V X5R 603
C7343 1UF 10% 16V X5R 603
C7344 1UF 10% 16V X5R 603
C7345 1UF 10% 16V X5R 603
C7346 1UF 10% 16V X5R 603
C7347 1UF 10% 16V X5R 603
C7348 1UF 10% 16V X5R 603
C7349 1UF 10% 16V X5R 603

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2016

PAGE TITLE: VREG: CPU CORE - PHASE 4

Apple Inc.

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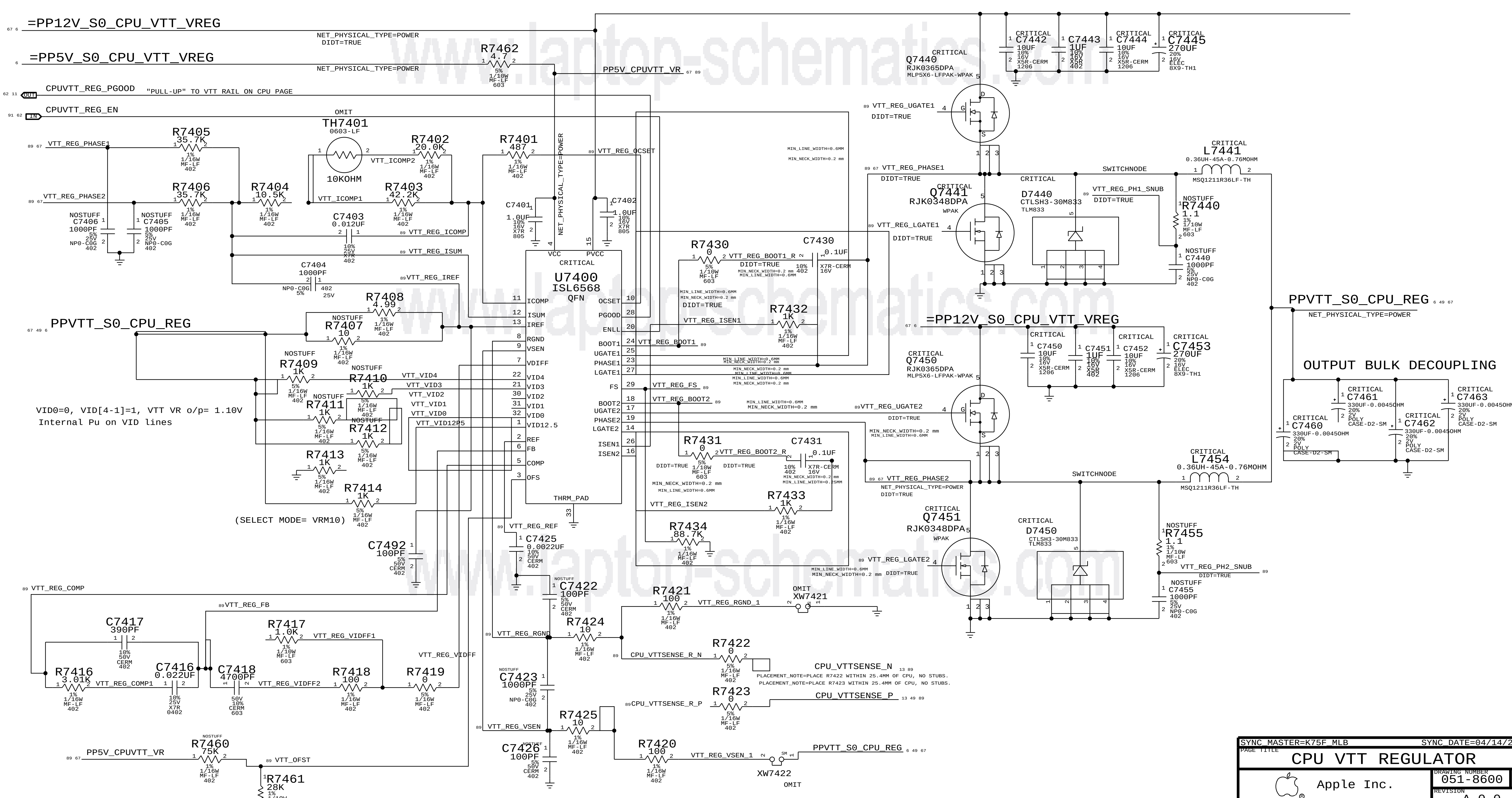
CPU VTT REG 1.1V/30A O/P= PPVTT_S0_CPU_REG

CPU VTT
VOUT = 1.1V OR 1.05V
PEAK = 35A
AVG = 30A



=PP12V_S0_CPU_VTT_VREG
=PP5V_S0_CPU_VTT_VREG
NET_PHYSICAL_TYPE=POWER
DIDT=TRUE
CPUVTT_REG_PGOOD
"PULL-UP" TO VTT RAIL ON CPU PAGE
CPUVTT_REG_EN
PP5V_CPUVTT_VR
VTT_REG_PHASE1
VTT_REG_PHASE2
VTT_REG_ICOMP
VTT_REG_ISUM
VTT_REG_IREF
VTT_REG_OCSET
TH7401
10KOHM
OMIT
R7405 35.7K
R7406 35.7K
R7404 10.5K
R7402 20.0K
R7403 42.2K
R7401 487
R7462 4.7
C7401 1.0UF
C7402 1.0UF
C7403 0.012UF
C7404 1000PF
C7405 1000PF
C7406 1000PF
U7400
ISL6568
QFN
CRITICAL
PPVTT_S0_CPU_REG
R7408 4.99
R7407 10
R7409 1K
R7410 1K
R7411 1K
R7412 1K
R7413 1K
R7414 1K
VTT_VID4
VTT_VID3
VTT_VID2
VTT_VID1
VTT_VID0
VTT_VID12P5
VID0=0, VID[4-1]=1, VTT VR o/p= 1.10V
Internal Pu on VID lines
(SELECT MODE= VRM10)
THRM_PAD
R7430 0
C7430 0.1UF
R7432 1K
R7431 0
C7431 0.1UF
R7433 1K
R7434 88.7K
VTT_REG_BOOT1_R
VTT_REG_BOOT2_R
VTT_REG_ISEN1
VTT_REG_ISEN2
VTT_REG_BOOT1
VTT_REG_BOOT2
VTT_REG_FS
VTT_REG_UGATE1
VTT_REG_LGATE1
VTT_REG_UGATE2
VTT_REG_LGATE2
Q7440 RJK0365DPA MLP5X6-LFPAK-WPAK
Q7441 RJK0348DPA WPAK
Q7450 RJK0365DPA MLP5X6-LFPAK-WPAK
Q7451 RJK0348DPA WPAK
D7440 CTLSH3-30M833 TLM833
D7450 CTLSH3-30M833 TLM833
L7441 0.36UH-45A-0.76MOHM MSQ1211R36LF-TH
L7454 0.36UH-45A-0.76MOHM MSQ1211R36LF-TH
SWITCHNODE
VTT_REG_PH1_SNUB
VTT_REG_PH2_SNUB
R7440 1.1
R7455 1.1
C7440 1000PF
C7455 1000PF
C7442 10UF
C7443 1UF
C7444 10UF
C7445 270UF
C7450 10UF
C7451 1UF
C7452 10UF
C7453 270UF
OUTPUT BULK DECOUPLING
C7460 330UF-0.0045OHM
C7461 330UF-0.0045OHM
C7462 330UF-0.0045OHM
C7463 330UF-0.0045OHM
VTT_REG_REF
C7425 0.0022UF
C7492 100PF
VTT_REG_COMP
VTT_REG_FB
C7417 390PF
R7416 3.01K
C7416 0.022UF
C7418 4700PF
R7417 1.0K
R7418 100
R7419 0
VTT_REG_VIDFF1
VTT_REG_VIDFF2
VTT_REG_VIDFF
VTT_REG_COMP1
C7422 100PF
R7424 10
C7423 1000PF
R7425 10
C7426 100PF
VTT_REG_RGND
VTT_REG_VSEN
R7421 100
VTT_REG_RGND_1
XW7421
R7422 0
R7423 0
CPU_VTTSENSE_R_N
CPU_VTTSENSE_R_P
CPU_VTTSENSE_N
CPU_VTTSENSE_P
PLACEMENT_NOTE=PLACE R7422 WITHIN 25.4MM OF CPU, NO STUBS.
PLACEMENT_NOTE=PLACE R7423 WITHIN 25.4MM OF CPU, NO STUBS.
R7420 100
VTT_REG_VSEN_1
XW7422
R7460 75K
R7461 28K
VTT_OFST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S0127	1	RES,68k,0603,5%	TH7401	

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: CPU VTT REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

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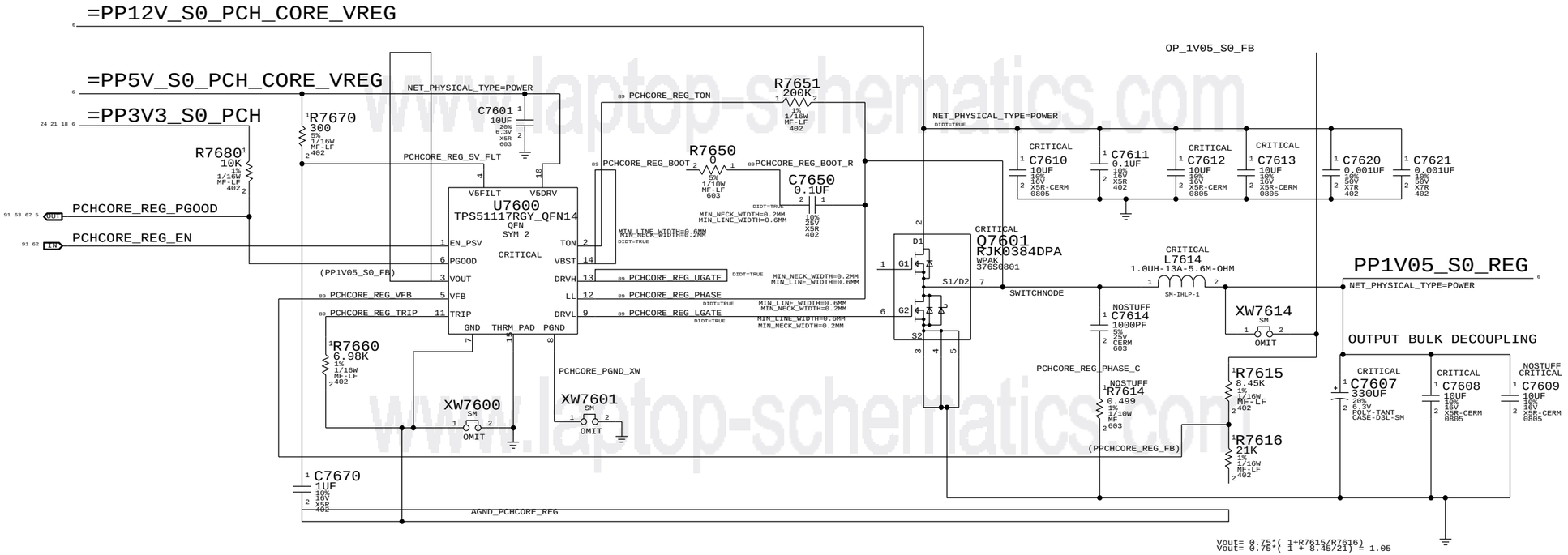
IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG
VOUT = 1.05V
PEAK = 7.5A
AVG = 3A



PAGE TITLE	IBEX PEAK CORE
Apple Inc.	DRAWING NUMBER 051-8600 · SIZE D
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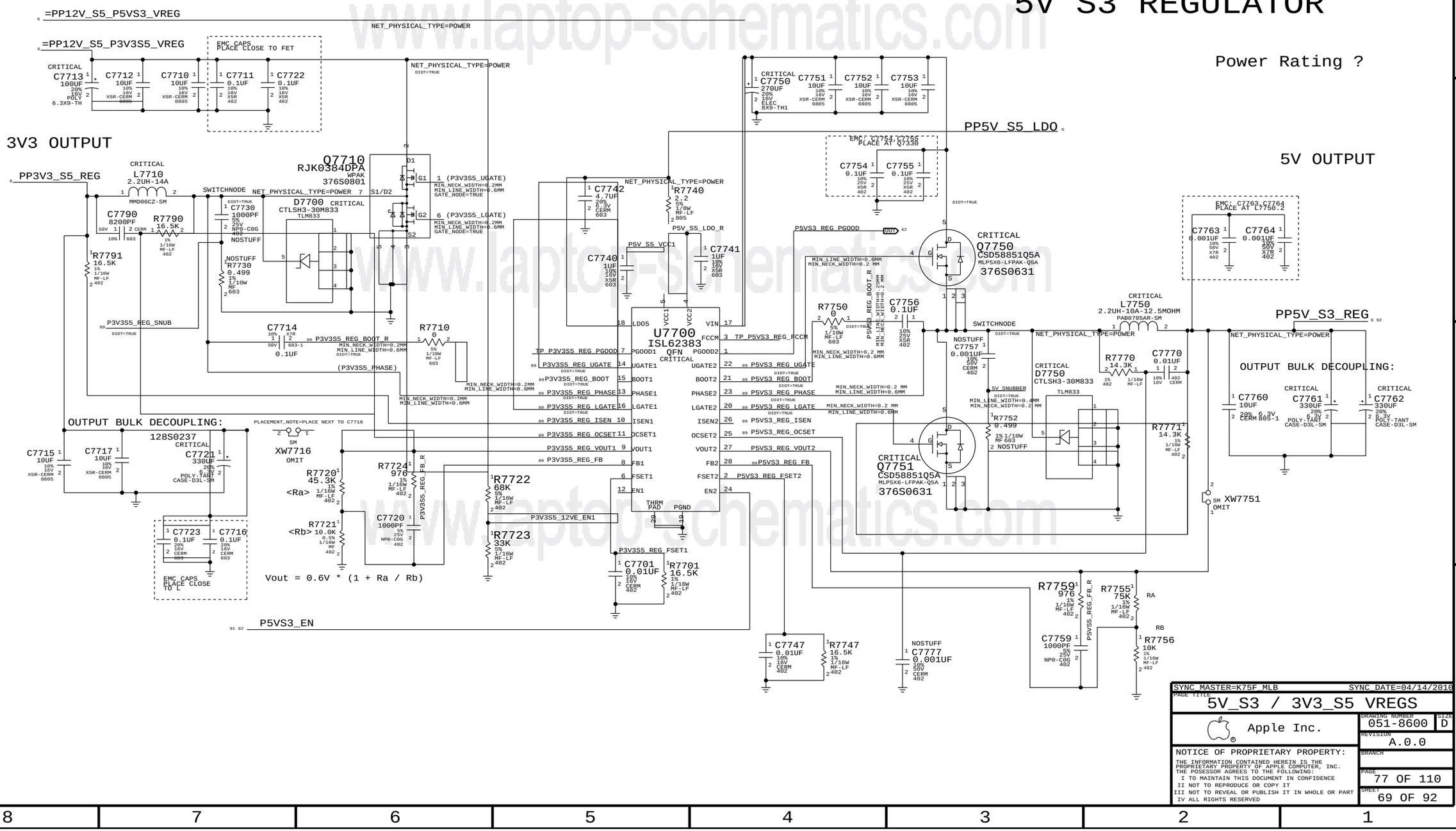
3V3 S5 REGULATOR

5V S3 REGULATOR



SYNC_MASTER=K75F MLB SYNC_DATE=04/14/2016

PAGE TITLE: 5V_S3 / 3V3_S5 VREGS

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

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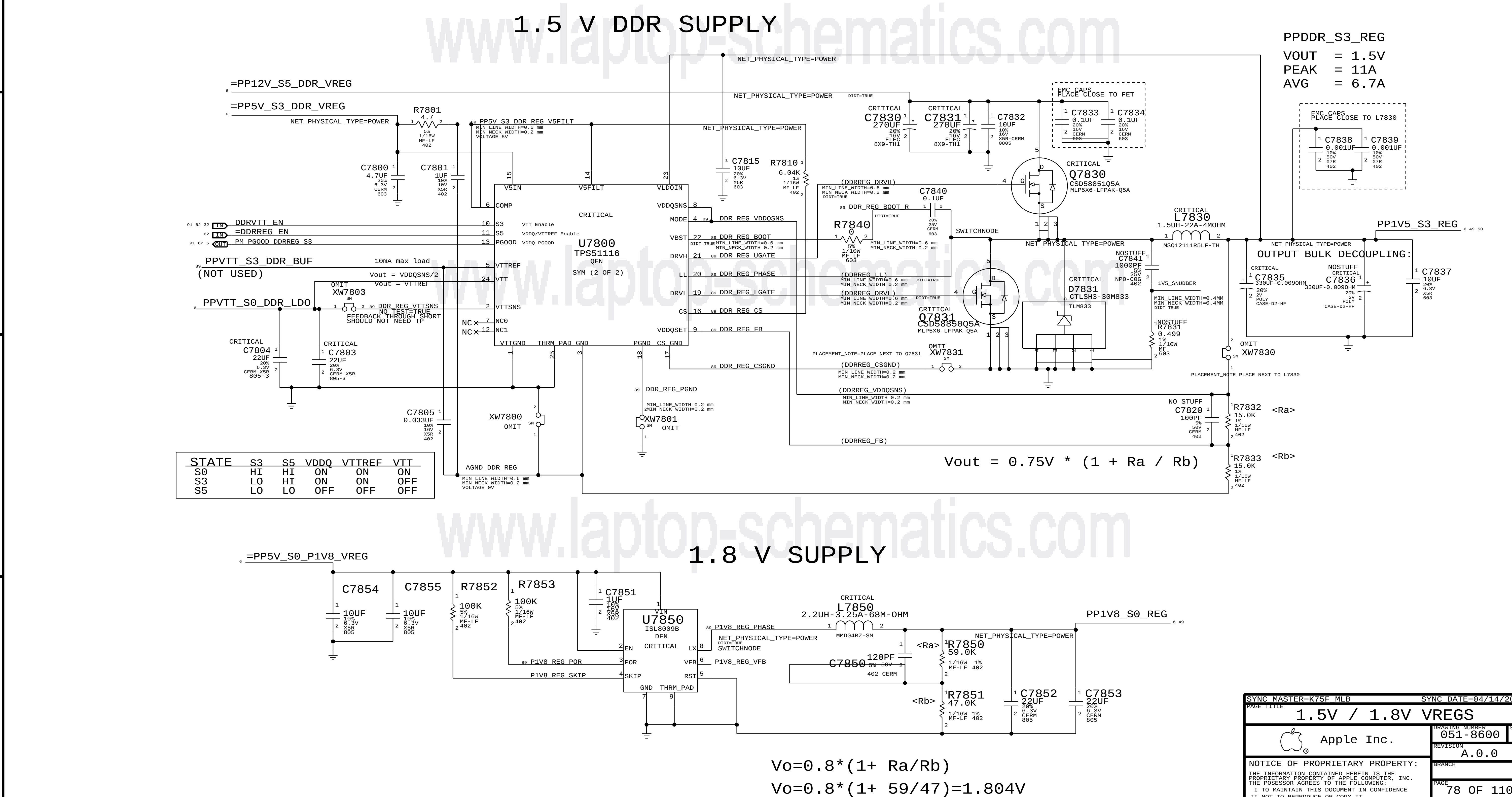


1.5 V DDR SUPPLY
=PP12V_S5_DDR_VREG
=PP5V_S3_DDR_VREG
NET_PHYSICAL_TYPE=POWER
R7801 4.7 5% 1/16W MF-LF 402
PP5V_S3_DDR_REG_V5FILT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C7800 4.7UF 20% 6.3V CERM 603
C7801 1UF 10% 10V X5R 402
C7815 10UF 20% 6.3V X5R 603
R7810 6.04K 1% 1/16W MF-LF 402
CRITICAL C7830 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7831 270UF 20% 16V ELEC 8X9-TH1
C7832 10UF 10% 16V X5R-CERM 0805
EMC CAPS PLACE CLOSE TO FET
C7833 0.1UF 20% 16V CERM 603
C7834 0.1UF 20% 16V CERM 603
PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A
EMC CAPS PLACE CLOSE TO L7830
C7838 0.001UF 10% 50V X7R 402
C7839 0.001UF 10% 50V X7R 402
CRITICAL Q7830 CSD58851Q5A MLP5X6-LFPAK-Q5A
(DDRREG_DRVH)
DDR_REG_BOOT_R
C7840 0.1UF 20% 25V CERM 603
R7840 0 5% 1/10W MF-LF 603
SWITCHNODE
CRITICAL L7830 1.5UH-22A-4MOHM MSQ12111R5LF-TH
PP1V5_S3_REG
DDRVTT_EN
=DDRREG_EN
PM_PGOOD_DDRREG_S3
V5IN V5FILT VLDOIN
COMP S3 S5 PGOOD
VTT Enable
VDDQ/VTTREF Enable
VDDQ PGOOD
CRITICAL U7800 TPS51116 QFN SYM (2 OF 2)
VDDQSNS MODE VBST DRVH LL DRVL CS VDDQSET
DDR_REG_VDDQSNS
DDR_REG_BOOT
DDR_REG_UGATE
DDR_REG_PHASE
DDR_REG_LGATE
DDR_REG_CS
DDR_REG_FB
PPVTT_S3_DDR_BUF
(NOT USED)
10mA max load
Vout = VDDQSNS/2
Vout = VTTREF
VTTREF VTT VTTSNS NC0 NC1
OMIT XW7803
DDR_REG_VTTSNS
NO_TEST=TRUE
FEEDBACK THROUGH SHORT
SHOULD NOT NEED TP
PPVTT_S0_DDR_LDO
VTTGND THRM_PAD GND PGND CS_GND
(DDRREG_LL)
(DDRREG_DRVL)
CRITICAL Q7831 CSD58850Q5A MLP5X6-LFPAK-Q5A
CRITICAL D7831 CTLSH3-30M833 TLM833
NOSTUFF C7841 1000PF 5% 25V NP0-C0G 402
1V5_SNUBBER
NOSTUFF R7831 0.499 1% 1/10W MF 603
OUTPUT BULK DECOUPLING:
CRITICAL C7835 330UF-0.009OHM 20% 2V POLY CASE-D2-HF
NOSTUFF CRITICAL C7836 330UF-0.009OHM 20% 2V POLY CASE-D2-HF
C7837 10UF 20% 6.3V X5R 603
CRITICAL C7804 22UF 20% 6.3V CERM-X5R 805-3
CRITICAL C7803 22UF 20% 6.3V CERM-X5R 805-3
PLACEMENT_NOTE=PLACE NEXT TO Q7831
OMIT XW7831
DDR_REG_CSGND
(DDRREG_CSGND)
OMIT XW7830
PLACEMENT_NOTE=PLACE NEXT TO L7830
(DDRREG_VDDQSNS)
DDR_REG_PGND
C7805 0.033UF 10% 16V X5R 402
XW7800 OMIT
XW7801 OMIT
NO STUFF C7820 100PF 5% 50V CERM 402
R7832 15.0K 1% 1/16W MF-LF 402 <Ra>
R7833 15.0K 1% 1/16W MF-LF 402 <Rb>
(DDRREG_FB)
Vout = 0.75V * (1 + Ra / Rb)
AGND_DDR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V
1.8 V SUPPLY
=PP5V_S0_P1V8_VREG
C7854 10UF 10% 6.3V X5R 805
C7855 10UF 10% 6.3V X5R 805
R7852 100K 5% 1/16W MF-LF 402
R7853 100K 5% 1/16W MF-LF 402
C7851 1UF 10% 16V X5R 402
U7850 ISL8009B DFN CRITICAL
VIN EN POR SKIP GND THRM_PAD LX VFB RSI
P1V8_REG_POR
P1V8_REG_SKIP
P1V8_REG_PHASE
NET_PHYSICAL_TYPE=POWER
DIDT=TRUE
SWITCHNODE
P1V8_REG_VFB
CRITICAL L7850 2.2UH-3.25A-68M-OHM MMD04BZ-SM
PP1V8_S0_REG
C7850 120PF 5% 50V 402 CERM
<Ra> R7850 59.0K 1/16W 1% MF-LF 402
<Rb> R7851 47.0K 1/16W 1% MF-LF 402
C7852 22UF 20% 6.3V CERM 805
C7853 22UF 20% 6.3V CERM 805
Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

1.5V / 1.8V VREGS

Apple Inc.

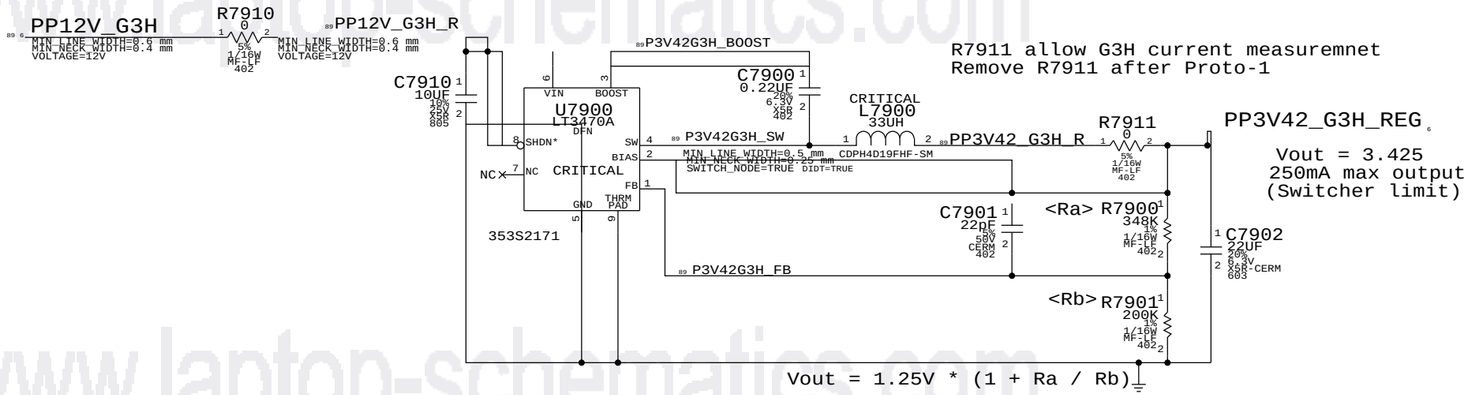
DRAWING NUMBER 051-8600 SIZE D

REVISION A.0.0

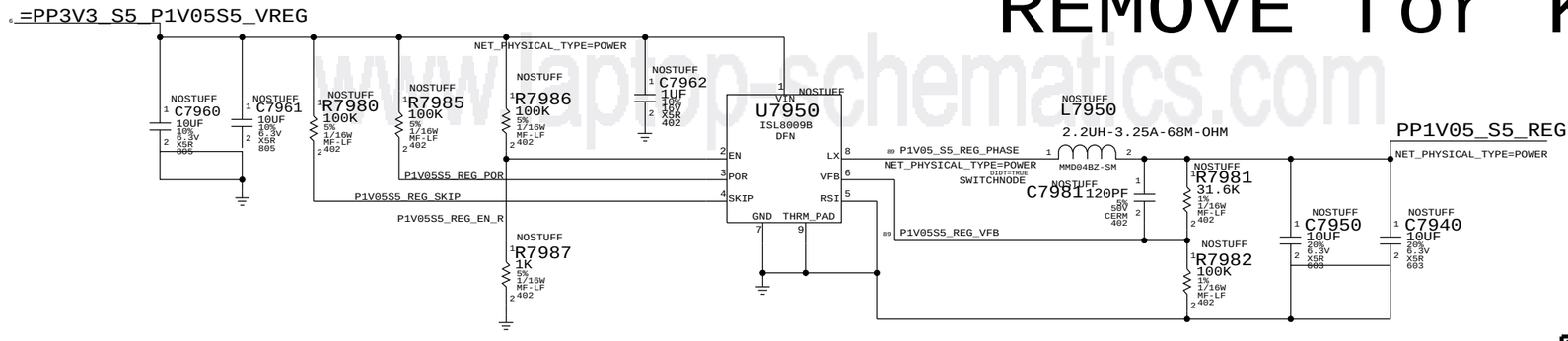
BRANCH

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



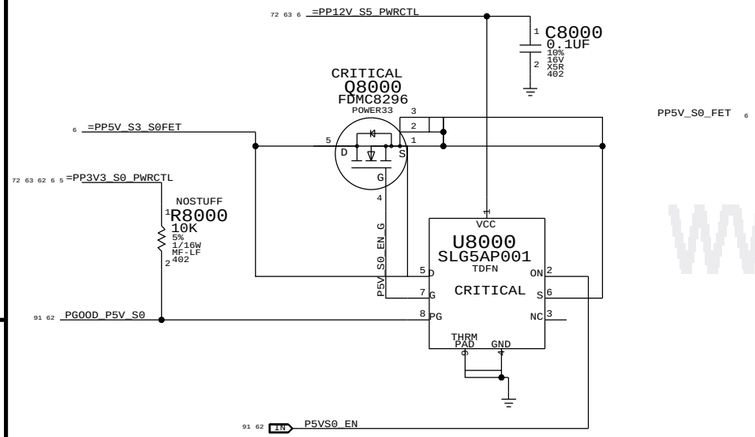
1.05V S5 SUPPLY



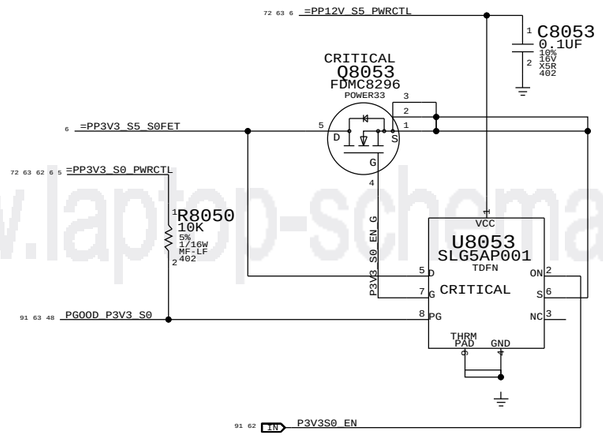
REMOVE for K60/K61

SYNC_MASTER=K75F_MLB	SYNC_DATE=04/14/2010
PAGE TITLE: 1.05 S5 SUPPLY	
Apple Inc.	DRAWING NUMBER: 051-8600 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 79 OF 110
	SHEET: 71 OF 92

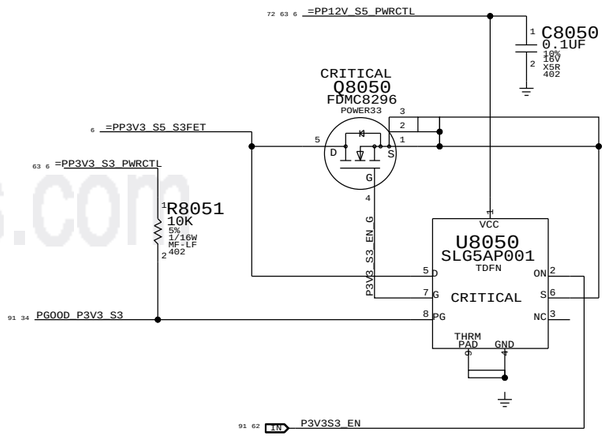
5V S0 FET (7A PK/2.7A AVG)



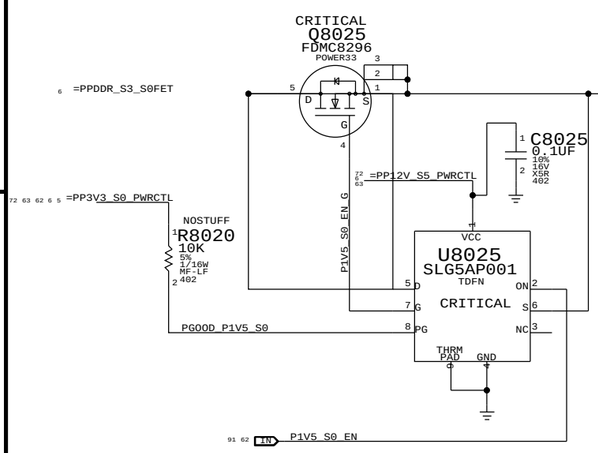
3.3V S0 FET (3.4APK / 1.9A AVG)



3.3V S3 FET (2.9A PK / 1.2A AVG)

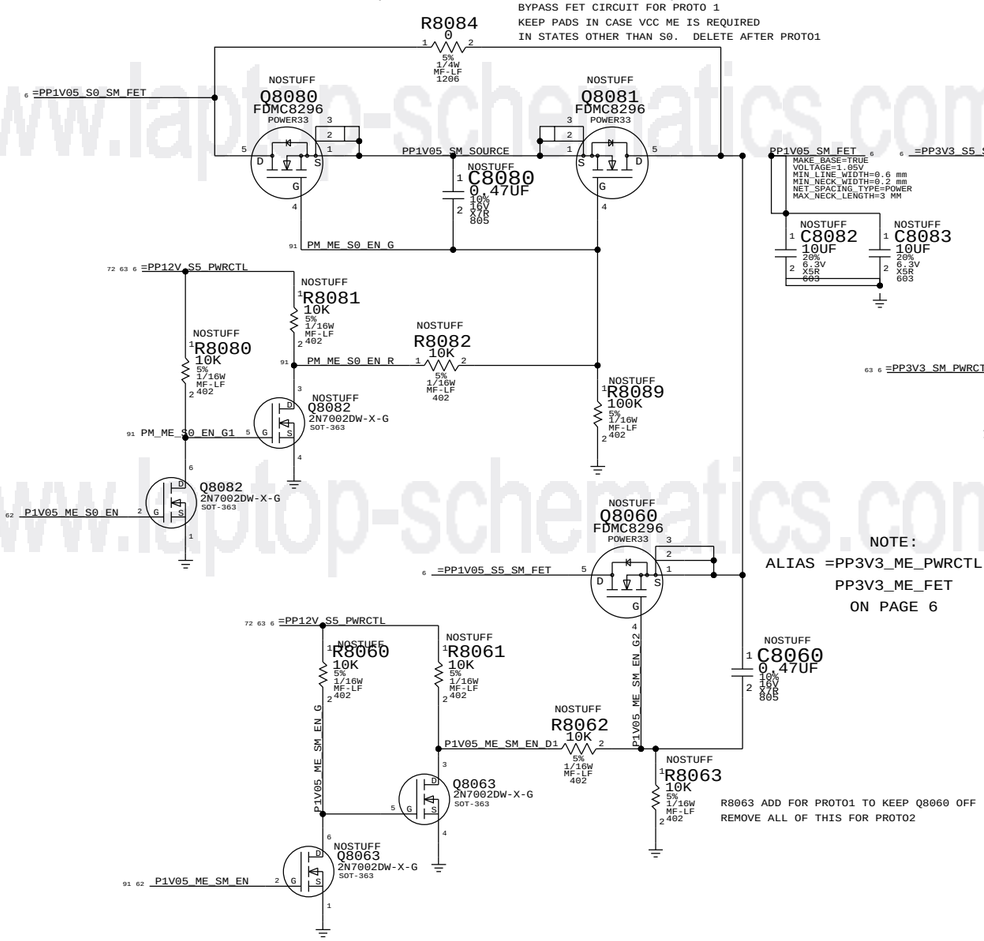


1.5V S0 FET (6.2A PK / 3A AVG)



1V05 ME FETS (S0: 2.2A MAX SM: 387MA)

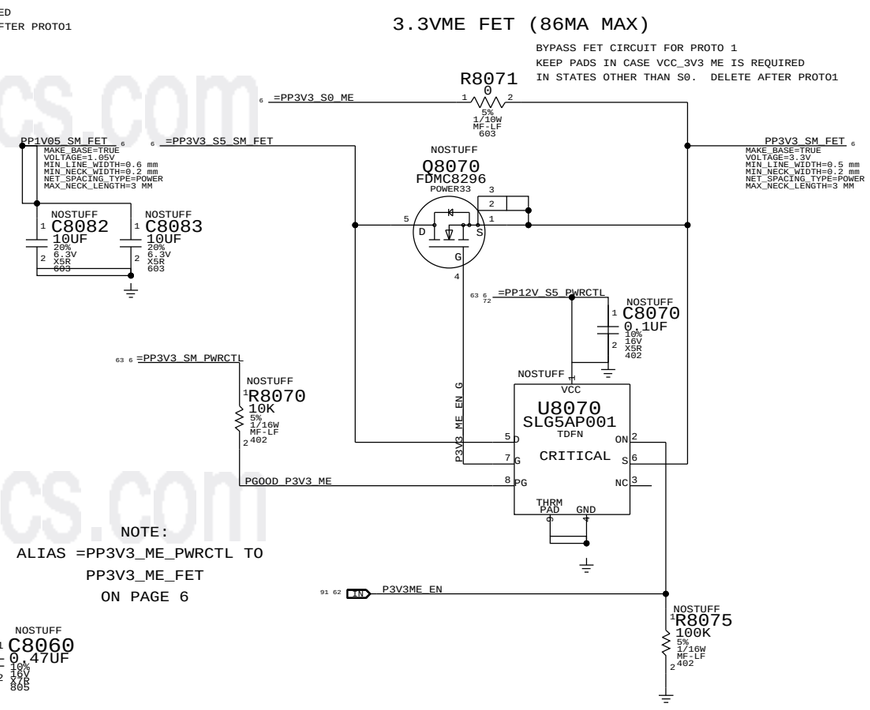
BYPASS FET CIRCUIT FOR PROTO 1
KEEP PADS IN CASE VCC ME IS REQUIRED
IN STATES OTHER THAN S0. DELETE AFTER PROTO1



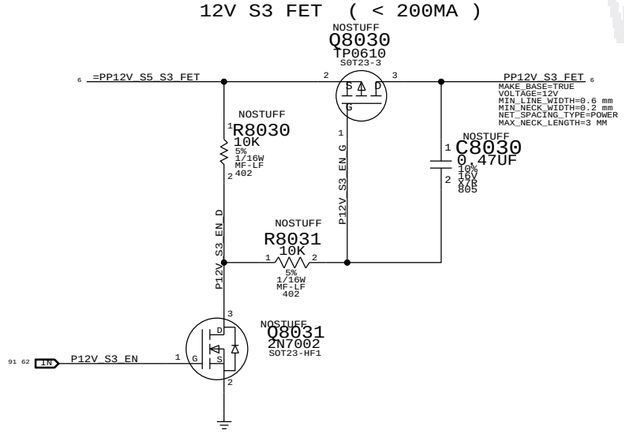
R8063 ADD FOR PROTO1 TO KEEP Q8060 OFF
REMOVE ALL OF THIS FOR PROTO2

3.3VME FET (86MA MAX)

BYPASS FET CIRCUIT FOR PROTO 1
KEEP PADS IN CASE VCC_3V3 ME IS REQUIRED
IN STATES OTHER THAN S0. DELETE AFTER PROTO1



12V S3 FET (< 200MA)



NOTE:
ALIAS =PP3V3_ME_PWRCTL TO
PP3V3_ME_FET
ON PAGE 6

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
S3+S0 FETS

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D
REVISION A.0.0
BRANCH
PAGE 80 OF 110
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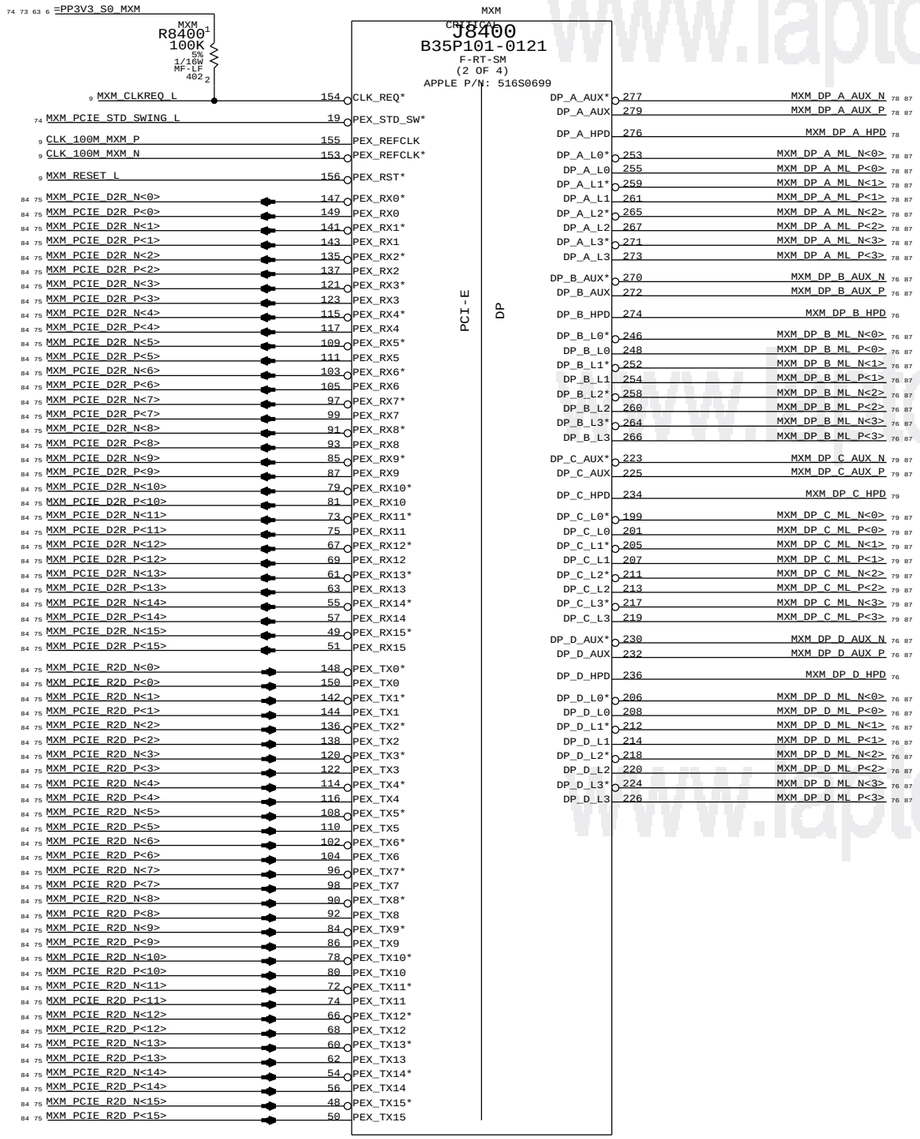
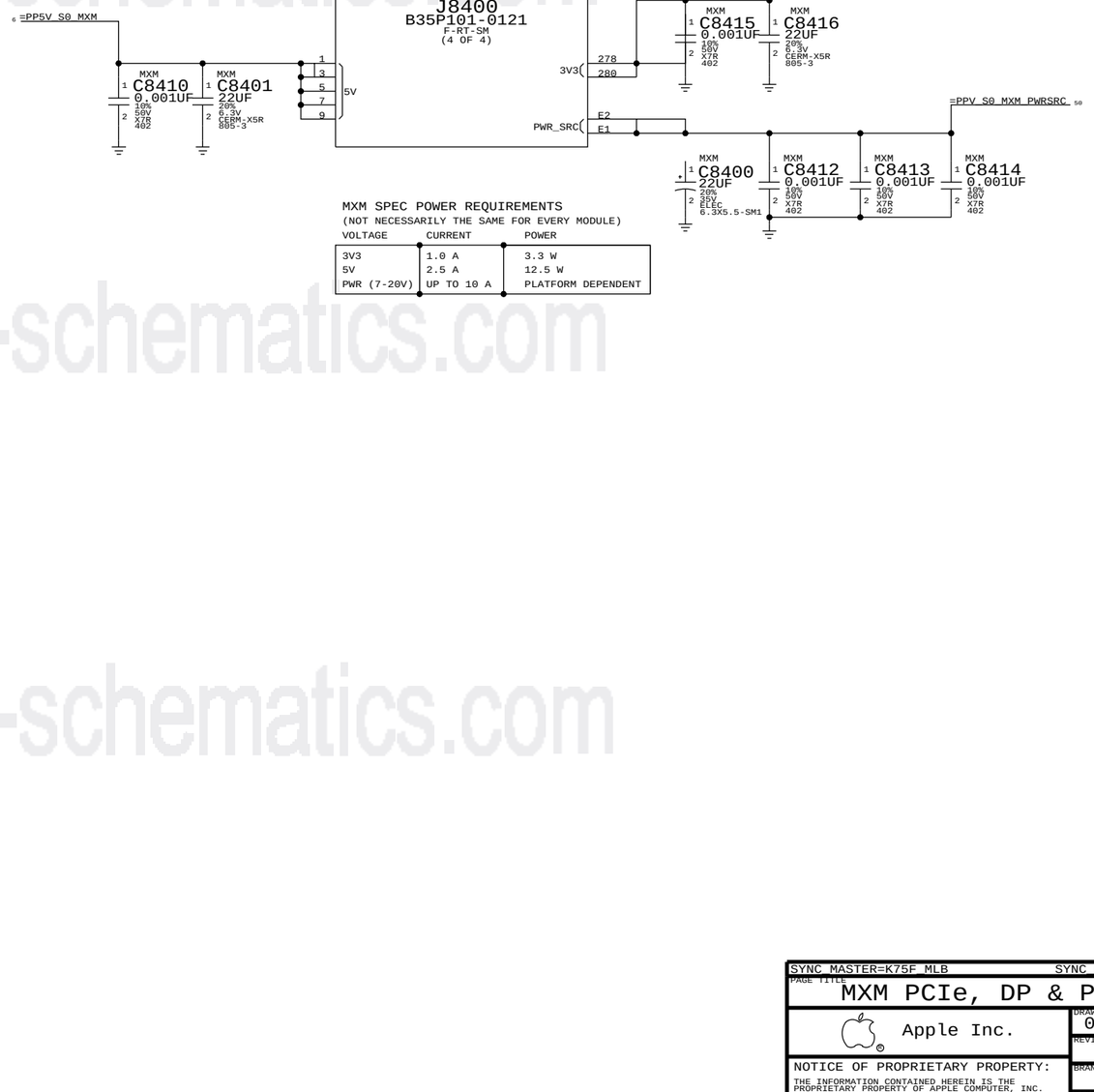
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 84 OF 110

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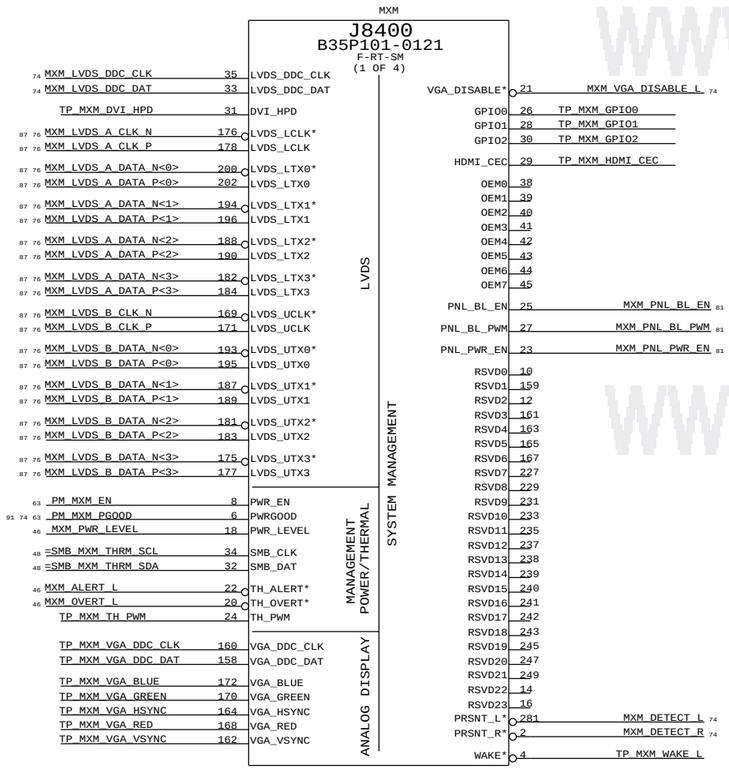
Page Notes

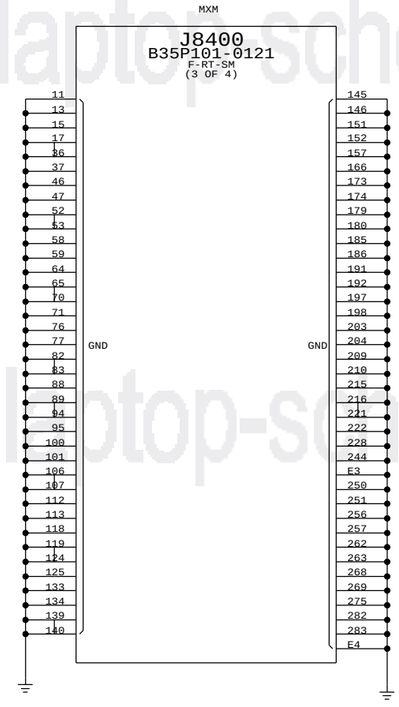
Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR





FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

NOSTUFF
R8510
0
MF-LF 5% 1/16W
402
MXM_VGA_DISABLE_L

FLOAT = LOW SWING
GND = HIGH SWING

NOSTUFF
R8504
0
MF-LF 5% 1/16W
402
MXM_PCIE_STD_SWING_L

=PP3V3_S0_MXM

R8500
100K
MF-LF 5% 1/16W
402
MXM_DETECT_L

PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT

R8501
100K
MF-LF 5% 1/16W
402
MXM_DETECT_R

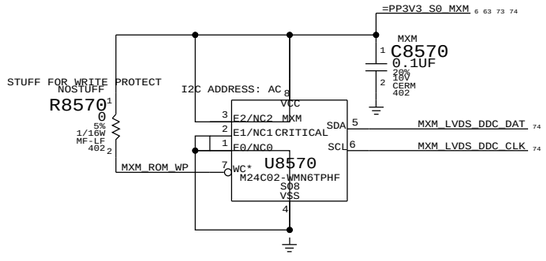
=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

R8503
10K
MF-LF 5% 1/16W
402
PM_MXM_PGOOD

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: MXM I/O

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D
REVISION: A.0.0
BRANCH:
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MXM TX CAPS

PEG_R2D_C_P<0>	MXM	C8600	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>
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MXM RX CAPS

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MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<11>
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SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 86 OF 110

SHEET: 75 OF 92

Page Notes

Power aliases required by this page:
- =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

87 74 MXM_LVDS_A_CLK_N — NC_MXM_LVDS_A_CLK_N
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_A_CLK_P — NC_MXM_LVDS_A_CLK_P
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_A_DATA_N<0> — NC_MXM_LVDS_A_DATA_N<0>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_A_DATA_P<0> — NC_MXM_LVDS_A_DATA_P<0>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_A_DATA_N<1> — NC_MXM_LVDS_A_DATA_N<1>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_A_DATA_P<1> — NC_MXM_LVDS_A_DATA_P<1>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_A_DATA_N<2> — NC_MXM_LVDS_A_DATA_N<2>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_A_DATA_P<2> — NC_MXM_LVDS_A_DATA_P<2>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_A_DATA_N<3> — NC_MXM_LVDS_A_DATA_N<3>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_A_DATA_P<3> — NC_MXM_LVDS_A_DATA_P<3>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_CLK_N — NC_MXM_LVDS_B_CLK_N
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_CLK_P — NC_MXM_LVDS_B_CLK_P
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_DATA_N<0> — NC_MXM_LVDS_B_DATA_N<0>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_DATA_P<0> — NC_MXM_LVDS_B_DATA_P<0>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_DATA_N<1> — NC_MXM_LVDS_B_DATA_N<1>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_DATA_P<1> — NC_MXM_LVDS_B_DATA_P<1>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_DATA_N<2> — NC_MXM_LVDS_B_DATA_N<2>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_DATA_P<2> — NC_MXM_LVDS_B_DATA_P<2>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_DATA_N<3> — NC_MXM_LVDS_B_DATA_N<3>
MAKE_BASE=TRUE NO_TEST=TRUE

87 74 MXM_LVDS_B_DATA_P<3> — NC_MXM_LVDS_B_DATA_P<3>
MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM DP Interfaces

87 73 MXM_DP_B_ML_P<0..3> — NC_MXM_DP_B_ML_P<0..3>
MAKE_BASE=TRUE NO_TEST=TRUE

87 73 MXM_DP_B_ML_N<0..3> — NC_MXM_DP_B_ML_N<0..3>
MAKE_BASE=TRUE NO_TEST=TRUE

87 73 MXM_DP_B_AUX_P — NC_MXM_DP_B_AUX_P
MAKE_BASE=TRUE NO_TEST=TRUE

87 73 MXM_DP_B_AUX_N — NC_MXM_DP_B_AUX_N
MAKE_BASE=TRUE NO_TEST=TRUE

73 MXM_DP_B_HPD — NC_MXM_DP_B_HPD
MAKE_BASE=TRUE NO_TEST=TRUE

87 73 MXM_DP_D_ML_P<0..3> — NC_MXM_DP_D_ML_P<0..3>
MAKE_BASE=TRUE NO_TEST=TRUE

87 73 MXM_DP_D_ML_N<0..3> — NC_MXM_DP_D_ML_N<0..3>
MAKE_BASE=TRUE NO_TEST=TRUE

87 73 MXM_DP_D_AUX_P — NC_MXM_DP_D_AUX_P
MAKE_BASE=TRUE NO_TEST=TRUE

87 73 MXM_DP_D_AUX_N — NC_MXM_DP_D_AUX_N
MAKE_BASE=TRUE NO_TEST=TRUE

73 MXM_DP_D_HPD — NC_MXM_DP_D_HPD
MAKE_BASE=TRUE NO_TEST=TRUE

Display: Aliases

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

APPLE INC.

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Page Notes

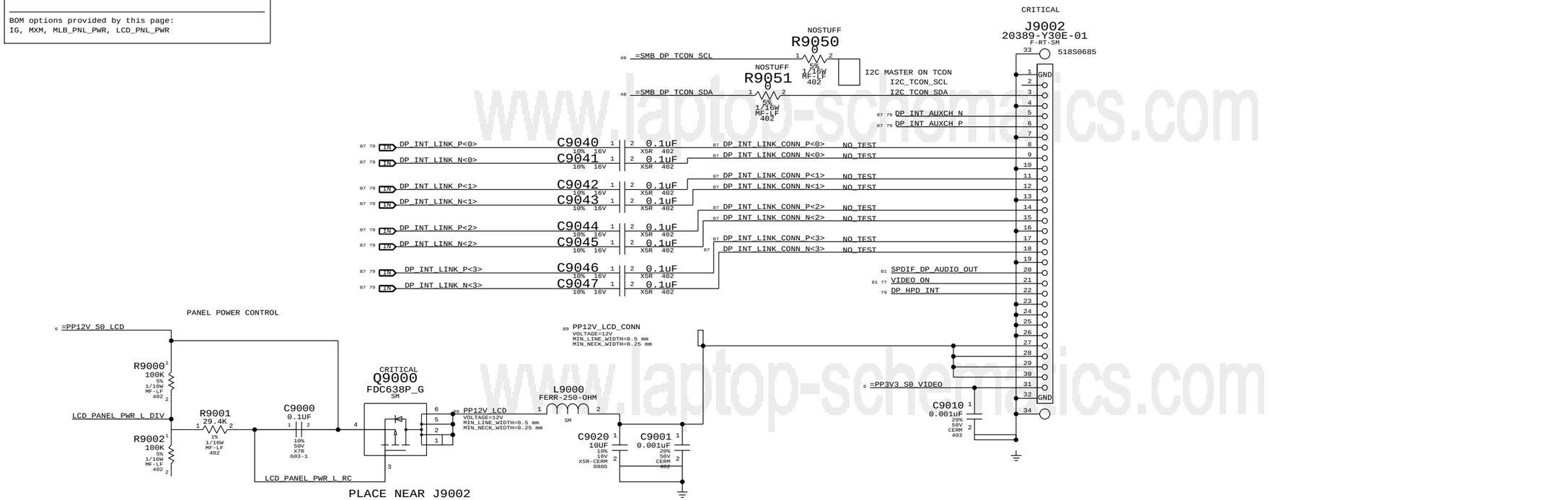
Power aliases required by this page:

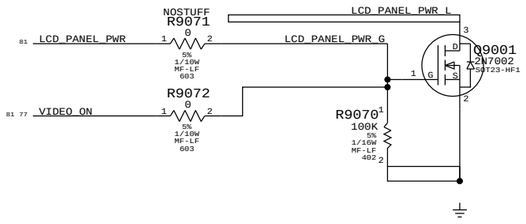
- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

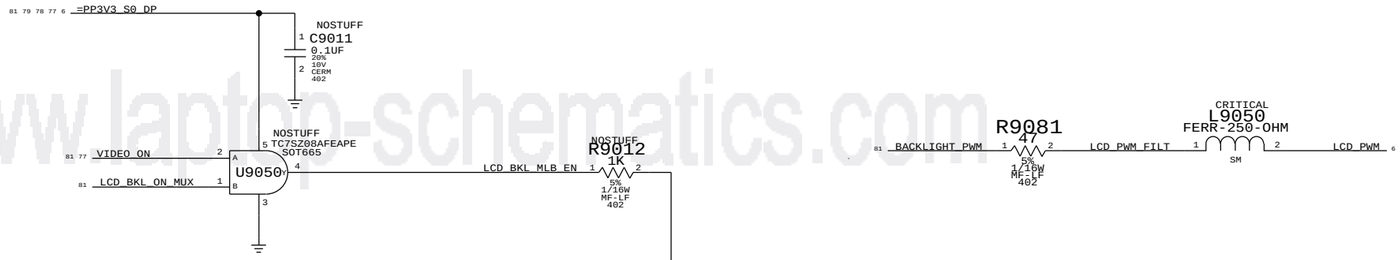
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

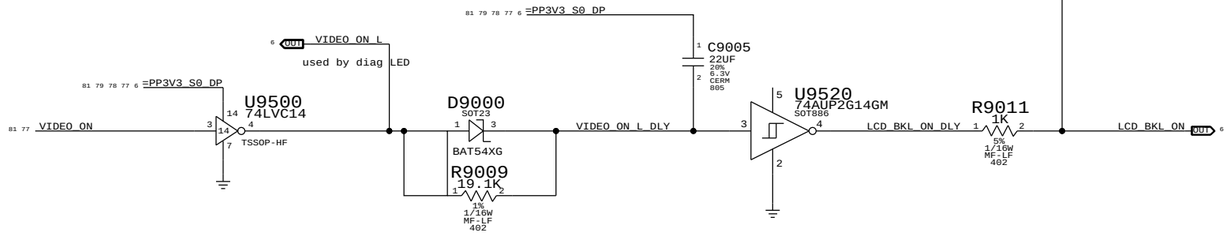






BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video
Options for GPU or MLB HW controlled backlight enable are included



buffers are multiple parts, other parts are on csa 95

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Display: Int DP Connector

Apple Inc.

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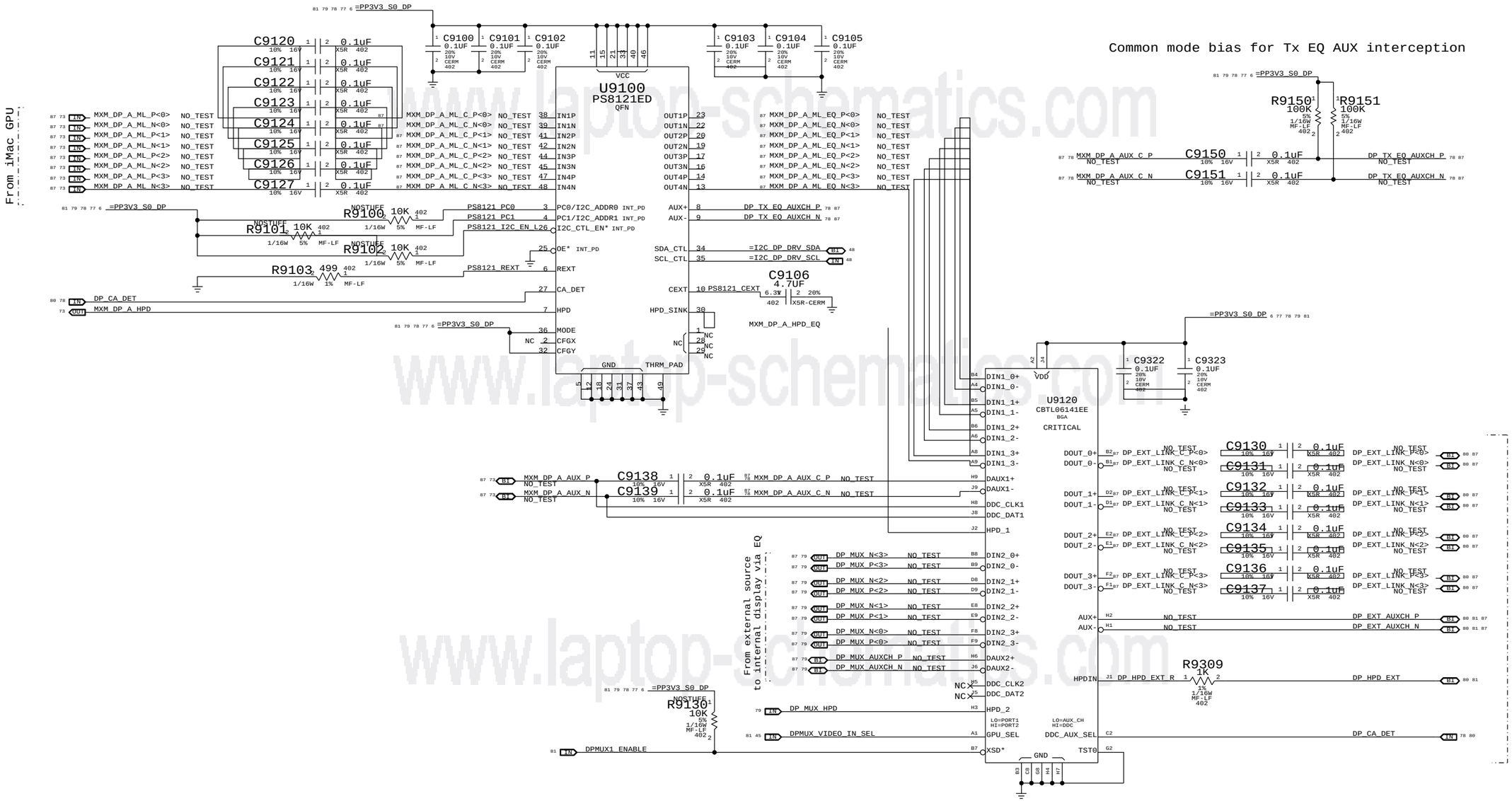
EQ & Re-Driver for DP source



DisplayPort Mux 1
Analog mux at External Connector

SYNC_MASTER=K75F_MLB	SYNC_DATE=04/14/2010
PAGE TITLE	Display: BiDiVi Mux1
Apple Inc.	DRAWING NUMBER 051-8600 · SIZE D
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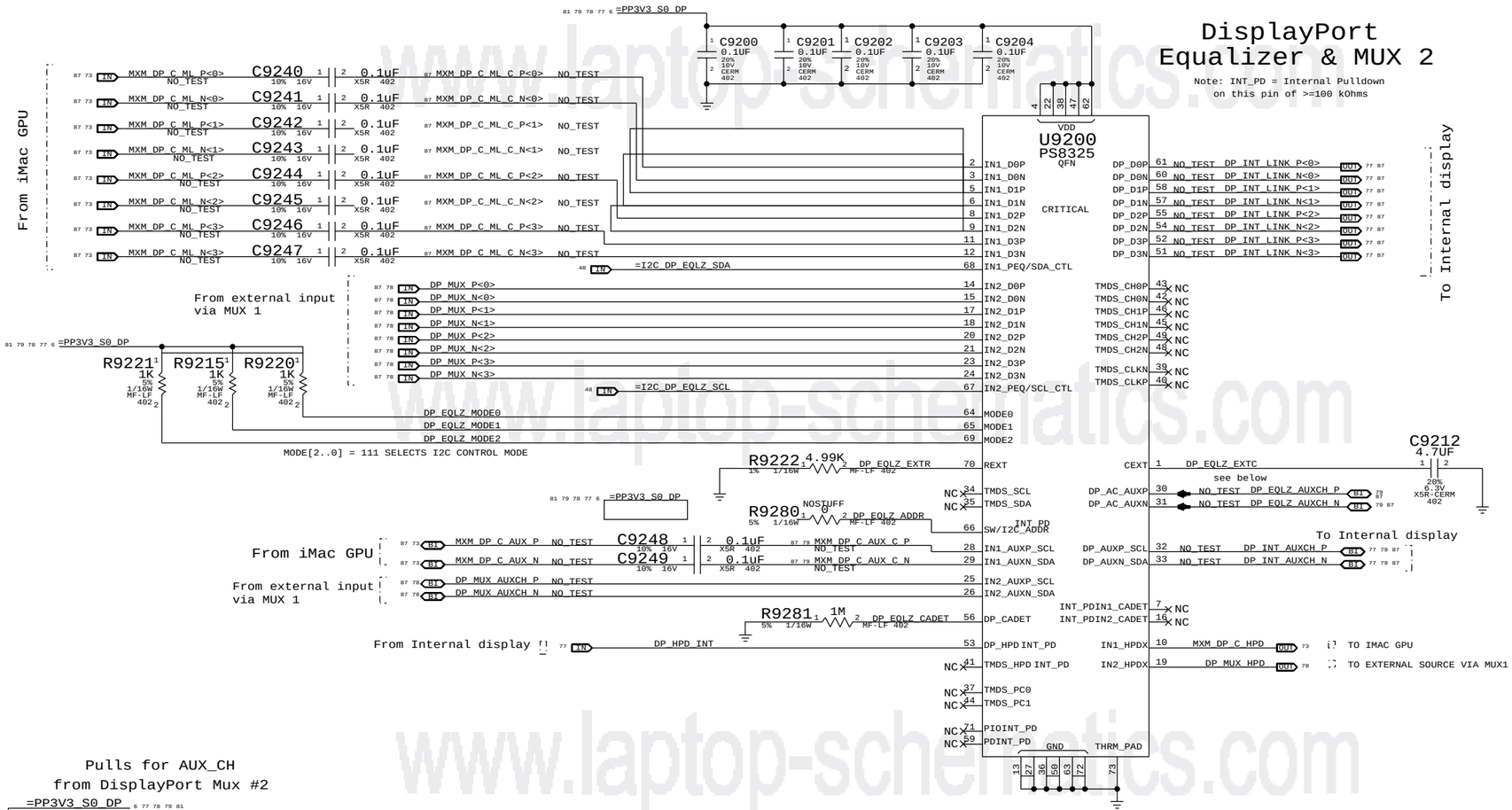
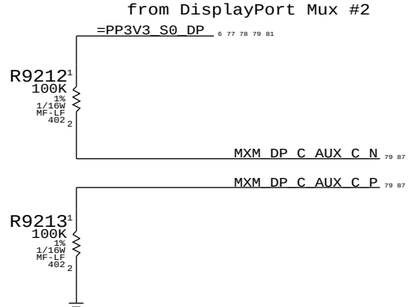
DisplayPort Equalizer & MUX 2

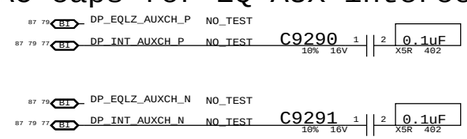
Note: INT_PD = Internal Pulldown on this pin of >=100 kOhms



Pulls for AUX_CH from DisplayPort Mux #2



AC caps for EQ AUX interception



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: BIDIVI DP MUX2

Apple Inc.

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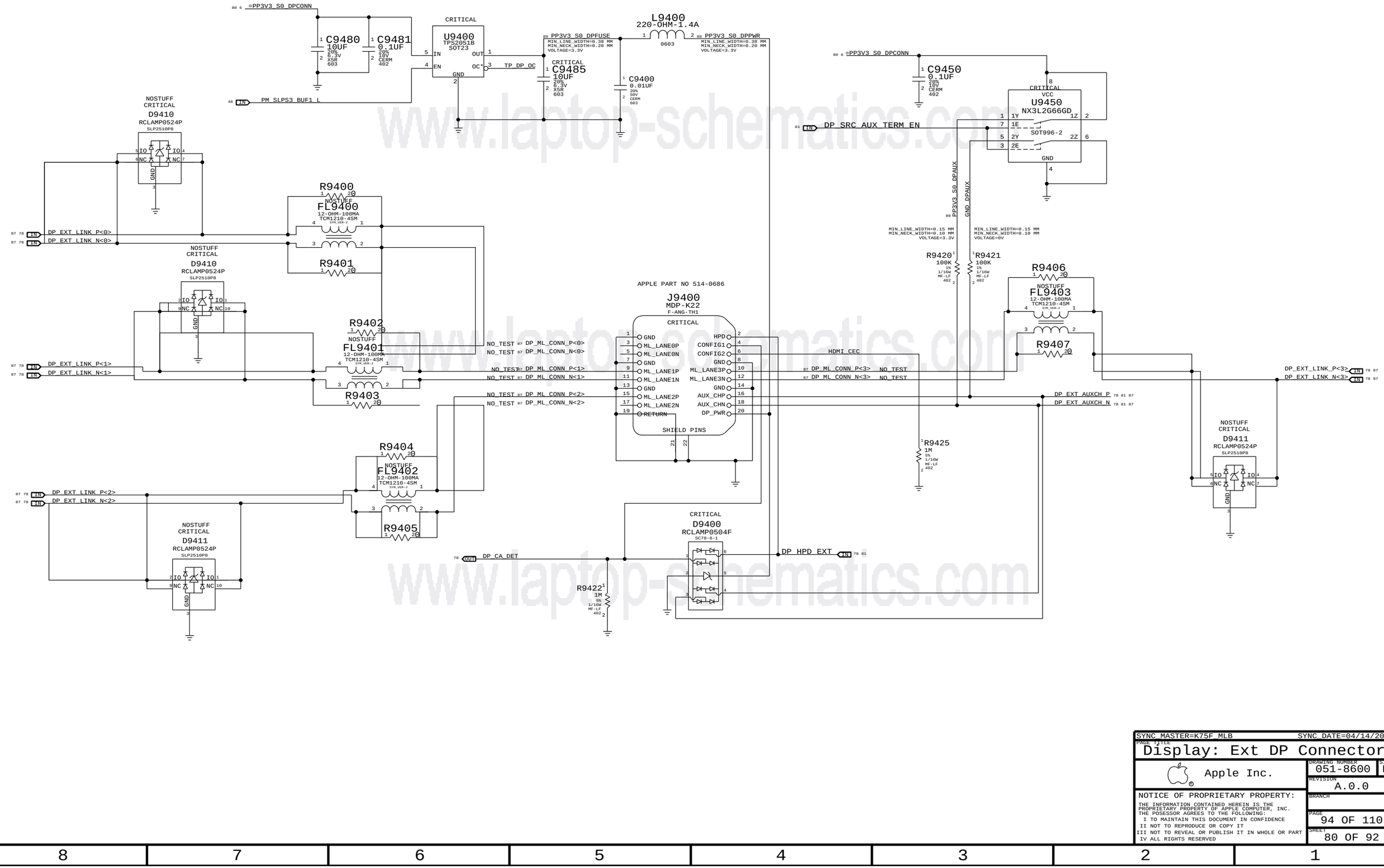

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

Display: Ext DP Connector

Apple Inc.

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PANEL/BACKLIGHT CONTROL MUX

=PP3V3_S0_DP
C9550 0.1UF 20% 16V CERM 402
U9500 74LVC14 TSSOP-HF
BIDIVI_AUX_TERM_EN
BIDIVI_AUX_TERM_EN_L
TC7SZ08AFEAPE SOT665
U9550
BIDIVI_BKL_MUX_SEL
DPMUX_VIDEO_IN_SEL
NOSTUFF R9523 0 5% 1/16W MF-LF 402
U9522 74LVC157A DHVQFN
BIDIVI_PWM
MXM_PNL_BL_PWM
BIDIVI_BKL_ON
MXM_PNL_BL_EN
BIDIVI_PNL_PWR_EN
MXM_PNL_PWR_EN
BACKLIGHT_PWM
LCD_BKL_ON_MUX
LCD_PANEL_PWR
THM GND PAD

DisplayPort AUDIO MUX

PLACE NEAR U6201

U9524 74LVC1G157 SOT886
SPDIF_DP_AUDIO_OUT
AUD_SPDIF_IN
AUD_SPDIF_IN_CODEC
R9542 0 5% 1/16W MF-LF 402
BIDIVI_AUDIO_MUX_SEL
NOSTUFF R9541 0 5% 1/16W MF-LF 402
AUD_MUX_CNTRL
MUX_CNTRL

BiDiVi MUX Enable

U9501 74LVC2G32 SOT902
DPMUX_VIDEO_IN_SEL
HPD_FILT
R9511 0 5% 1/16W MF-LF 402
DPMUX1_OROUT_L
DPMUX1_ENABLE

*Some inputs listed below come up as outputs driven low under the SMC flasher
Series R should prevent any issues on the inputs
Ouptuts are OK as low by default

SMC Signals for BiDiVi

R9510 3.3K 5% 1/16W MF-LF 402
VIDEO_ON
SMC_VIDEO_ON
AUXCH_P_STATE
AUXCH_N_STATE
SMC_DP_HPD
R9540 3.3K 5% 1/16W MF-LF 402
MXM_PNL_BL_PWM
SMC_PNL_BL_PWM

Inputs	SMC		Outputs	S5/S3	S0
	P21*	P27	DPMUX_VIDEO_IN_SEL	0	0
	P22*	PF3	BIDIVI_AUX_TERM_EN	0	0
	P23*	PF4	BIDIVI_PNL_PWR_EN	0	0
	P25*	PF6	BIDIVI_BKL_ON	X	X
		PF7	BIDIVI_BKL_PWM	X	X
	PG0	P26	BIDIVI_AUDIO_MUX_SEL	0	0

External AUX Channel and HPD Buffers & filters

=PP3V3_S0_DP
CRITICAL
U9540 NX3L1G66 SOT886
DP_SINK_AUX_TERM_EN
C9500 0.1UF 20% 16V CERM 402
R9543 499K 1% 1/16W MF-LF 402
PP3V3_S0_DPAUXP_SINK
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.15 MM
MIN_NECK_WIDTH=0.10 MM
DP_EXT_AUXCH_P
R9520 4.75M 1% 1/16W MF 402
U9510 74AUP2G14GM SOT886
D9500 SOT23 BAT54XG
R9502 1K 5% 1/16W MF-LF 402
C9501 1UF 10% 6.3V CERM 402
U9500 74LVC14 TSSOP-HF
R9503 3.3K 5% 1/16W MF-LF 402
DP_AUXP_L
DP_AUXP_DLY_L
AUXCH_P_STATE
DP_EXT_AUXCH_N
R9521 4.75M 1% 1/16W MF 402
D9501 SOT23 BAT54XG
R9505 1K 5% 1/16W MF-LF 402
C9503 1UF 10% 6.3V CERM 402
R9506 3.3K 5% 1/16W MF-LF 402
DP_AUXN_L
DP_AUXN_DLY_L
AUXCH_N_STATE
D9503 SOT23 BAT54XG
PP3V3_S0_DP_D
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.15 MM
MIN_NECK_WIDTH=0.10 MM
C9562 0.1UF 20% 16V CERM 402
U9520 74AUP2G14GM SOT886
DP_HPD_EXT
R9507 1M 5% 1/16W MF-LF 402
DP_HPD_EXT_L
D9502 SOT23 BAT54XG
R9508 4.7K 5% 1/16W MF-LF 402
DP_HPD_PULS_EAT_L
C9504 1UF 10% 6.3V CERM 402
R9509 3.3K 5% 1/16W MF-LF 402
SMC_DP_HPD
HPD_FILT

AUX Bias Enable

U9500 74LVC14 TSSOP-HF
DPMUX_VIDEO_IN_SEL
DPMUX_VIDEO_IN_SEL_L
U9502 74LVC2G08 SOT902
DP_SRC_AUX_TERM_EN
enables 100k dp aux source termination
C9560 0.1UF 20% 16V CERM 402
C9561 0.1UF 20% 16V CERM 402
U9501 74LVC2G32 SOT902
HPD_FILT
BIDIVI_AUX_TERM_EN
AUX_TERM_OR_OUT
enables weak sink-like aux termination
so that one bi-directional system can find the other
DP_SINK_AUX_TERM_EN

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: Display: BiDiVi Support

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D
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K60/K61 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.085 MM	=STANDARD		
35_OHM_SE	*	Y	0.19 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD		
39_OHM_SE	*	Y	0.16 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD		
45_OHM_SE	*	Y	0.12 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

K60/K61 RULE DEFINITIONS

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8600	3.0.0

SCALE	SHT	OF
NONE	82	92

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_35S	*	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_ODD2DQ_ODD	*	=3:1_SPACING	?
MEM_DQ_ODD2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_EVEN	*	=3:1_SPACING	?
MEM_DQ_EVEN2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_ODD	*	=5:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_ODD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_EVEN	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_ODD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_EVEN	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_ODD	MEM_CLK	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CTRL	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CMD	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_ODD	*	MEM_DQ_ODD2DQ_ODD
MEM_DQ_ODD	MEM_DQS	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_EVEN	MEM_CLK	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CTRL	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CMD	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_EVEN
MEM_DQ_EVEN	MEM_DQS	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_ODD	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_ODD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_EVEN	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DQ_ODD	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
MEM_CMD	MEM_DQ_EVEN	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DQ_ODD	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER
MEM_DQ_EVEN	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_RCOMP_PHY	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_CLK	MEM_A_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_A_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_A<15..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_BA<2..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_RAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_CAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_WE_L	12 30
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_A<15..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_BA<2..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_RAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_CAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_WE_L	12 31
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<7>	12 32

MEMORY POWER PROPERTIES

NET_TYPE VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1.5S	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A	12 28
1.5S	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B	12 28
1.66	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMA_DQ	28
1.67	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMB_DQ	28
1.66	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A_SW	28
1.66	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B_SW	28

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	12 32
1.5D	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP0	11
1.5D	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP1	11
1.5D	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP2	11
1.67	MEM_70D	MEM_DQS	TP_MEM_B_DQS_P<8>	8 12
1.67	MEM_70D	MEM_DQS	TP_MEM_B_DQS_N<8>	8 12
1.67	MEM_70D	MEM_DQS	TP_MEM_A_DQS_P<8>	8 12
1.67	MEM_70D	MEM_DQS	TP_MEM_A_DQS_N<8>	8 12

ADD RULES TO NC_DQS<8>
TO CLEAR CHECK_PLUS ERRORS

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FDI_MISC			
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>
	CPU_50S	CPU_AGTL	FDI_INT
SATA SSD			
	SATA_85D	SATA	SATA_SSD_R2D_C_P 18 42
	SATA_85D	SATA	SATA_SSD_R2D_C_N 18 42
	SATA_85D	SATA	SATA_SSD_R2D_P 42
	SATA_85D	SATA	SATA_SSD_R2D_N 42
	SATA_85D	SATA	SATA_SSD_D2R_P 18 42
	SATA_85D	SATA	SATA_SSD_D2R_N 18 42
	SATA_85D	SATA	SATA_SSD_D2R_C_P 42
	SATA_85D	SATA	SATA_SSD_D2R_C_N 42
CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_P 10 18
	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_N 10 18
CPU ITP			
	CPU_50S	CPU_ITP	XDP_BPM_L<7..0> 11 25
	CPU_50S	CPU_ITP	CPU_CFG<17..0> 10 15 25
	CPU_50S	CPU_ITP	XDP_OBSDATA_A<3..0> 25
CPU_MISC			
	CPU_50S	CPU_RCOMP	CPU_PEG_COMP 10
	CPU_50S	CPU_RCOMP	CPU_PEG_RBIAS 10
	CPU_50S	CPU_RCOMP	CPU_COMP3 11
	CPU_50S	CPU_RCOMP	CPU_COMP2 11
	CPU_50S	CPU_RCOMP	CPU_COMP1 11
	CPU_50S	CPU_RCOMP	CPU_COMP0 11

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCIE GRAPHICS			
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0> 9 75
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0> 9 75
	PCIE_85D	PCIE	PEG_D2R_P<15..0> 9 75
	PCIE_85D	PCIE	PEG_D2R_N<15..0> 9 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<15..0> 73 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<15..0> 73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<15..0> 73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<15..0> 73 75
PCIE I/O			
	PCIE_85D	PCIE	PCIE_MINI_R2D_P 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P 18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N 18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P 18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N 18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_P 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_N 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P 39
	PCIE_85D	PCIE	PCIE_FW_R2D_N 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P 18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N 18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P 18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N 18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N 39
DMI			
	PCIE_85D	PCIE	DMI_S2N_P<3..0> 10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0> 10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0> 10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0> 10 19
FDI			
	PCIE_85D	PCIE	FDI_DATA_N<7..0>
	PCIE_85D	PCIE	FDI_DATA_P<15..0>
PCIE REF CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P 9
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N 9
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P 18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N 18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P 18 39
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N 18 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P 18 36
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N 18 36
SATA			
	SATA_85D	SATA	SATA_HDD_R2D_C_P 18 42
	SATA_85D	SATA	SATA_HDD_R2D_C_N 18 42
	SATA_85D	SATA	SATA_HDD_R2D_P 42 92
	SATA_85D	SATA	SATA_HDD_R2D_N 42 92
	SATA_85D	SATA	SATA_HDD_D2R_P 18 42
	SATA_85D	SATA	SATA_HDD_D2R_N 18 42
	SATA_85D	SATA	SATA_HDD_D2R_C_P 42 92
	SATA_85D	SATA	SATA_HDD_D2R_C_N 42 92
	SATA_85D	SATA	SATA_ODD_R2D_C_P 18 42
	SATA_85D	SATA	SATA_ODD_R2D_C_N 18 42
	SATA_85D	SATA	SATA_ODD_R2D_P 42 92
	SATA_85D	SATA	SATA_ODD_R2D_N 42 92
	SATA_85D	SATA	SATA_ODD_D2R_P 18 42
	SATA_85D	SATA	SATA_ODD_D2R_N 18 42
	SATA_85D	SATA	SATA_ODD_D2R_C_P 42 92
	SATA_85D	SATA	SATA_ODD_D2R_C_N 42 92
CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_P 11 21
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_N 11 21
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_P 11 18
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_N 11 18
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_P 11 25
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_N 11 25
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_P 11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_N 11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_P 18 26
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_N 18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_P 18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_N 18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_P 18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_N
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_P 18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_N 18 26

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PAGE TITLE

PCIE/DMI/FDI/SATA CONSTRAINTS

Apple Inc.

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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	0.2 MM	?
COMP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_55S	PCI	PCI_REQ0_L	20
	PCI_55S	PCI	PCI_REQ1_L	20
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	20 27
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	18 27
	LPC_55S	LPC	LPC_AD<3..0>	18 45 47
	LPC_55S	LPC	LPC_FRAME_L	18 45 47
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	20 27
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	27 45
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	27 47
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK_R	9 19 91
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK	9 45 91
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 27
	USB_90D	USB	USB_EXTA_P	34 43
	USB_90D	USB	USB_EXTA_N	34 43
	USB_90D	USB	USB_PORT0_P	43
	USB_90D	USB	USB_PORT0_N	43
	USB_90D	USB	USB_EXTB_P	35 43
	USB_90D	USB	USB_EXTB_N	35 43
	USB_90D	USB	USB_PORT1_P	43
	USB_90D	USB	USB_PORT1_N	43
	USB_90D	USB	USB_EXTC_P	34 43
	USB_90D	USB	USB_EXTC_N	34 43
	USB_90D	USB	USB_PORT2_P	43
	USB_90D	USB	USB_PORT2_N	43
	USB_90D	USB	USB_EXTD_P	35 43
	USB_90D	USB	USB_EXTD_N	35 43
	USB_90D	USB	USB_D_MUXED_P	43
	USB_90D	USB	USB_D_MUXED_N	43
	USB_90D	USB	USB_PORT3_P	43
	USB_90D	USB	USB_PORT3_N	43
	USB_90D	USB	USB_CAMERA_P	34 44
	USB_90D	USB	USB_CAMERA_N	34 44
	USB_90D	USB	USB_CAMERA_L_P	44 92
	USB_90D	USB	USB_CAMERA_L_N	44 92
	USB_90D	USB	USB_BT_P	35 44
	USB_90D	USB	USB_BT_N	35 44
	USB_90D	USB	USB_BT_L_P	44 92
	USB_90D	USB	USB_BT_L_N	44 92
	USB_90D	USB	USB_IR_P	34 44
	USB_90D	USB	USB_IR_N	34 44
	USB_90D	USB	USB_IR_L_P	44 92
	USB_90D	USB	USB_IR_L_N	44 92
	USB_90D	USB	USB_SDCARD_P	35 44
	USB_90D	USB	USB_SDCARD_N	35 44
	USB_90D	USB	USB_SDCARD_L_P	44 92
	USB_90D	USB	USB_SDCARD_L_N	44 92
	USB_90D	USB	USB_WM_P	20 44
	USB_90D	USB	USB_WM_N	20 44
	USB_90D	USB	USB_WM_L_P	44
	USB_90D	USB	USB_WM_L_N	44
	USB_90D	USB	USB_MINI_P	
	USB_90D	USB	USB_MINI_N	
	USB_90D	USB	USB_BRCRYPT_P	20 44
	USB_90D	USB	USB_BRCRYPT_N	20 44
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 27
	CLK_XTAL	XTAL	CK505_XTAL_IN	26
	CLK_XTAL	XTAL	CK505_XTAL_OUT	26
	CLK_PCH_55S	CLK_PCH	PCH_CLK14P3M_REFCLK	18 26
	USB_90D	USB	USB_BRCRYPT_L_P	44
	USB_90D	USB	USB_BRCRYPT_L_N	44
	USB_90D	USB	USB_HUB1_UP_P	20 34
	USB_90D	USB	USB_HUB1_UP_N	20 34
	USB_90D	USB	USB_HUB2_UP_P	20 35
	USB_90D	USB	USB_HUB2_UP_N	20 35

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SPI_55S	SPI	SPI_CLK_R	18 47 54
	SPI_55S	SPI	SPI_CLK	54
	SPI_55S	SPI	SPI_MOSI_R	18 47 54
	SPI_55S	SPI	SPI_MOSI	54
	SPI_55S	SPI	SPI_MISO	18 47 54
	SPI_55S	SPI	SPI_MISO_R	54
	SPI_55S	SPI	SPI_CS0_R_L	18 47
	SPI_55S	SPI	SPI_CS0_L	47
	SPI_55S	SPI	SPI_MLB_CS_L	47 54
	SPI_55S	SPI	SPI_ALT_CS_L	47
	SPI_55S	SPI	SPIROM_USE_MLB	21 47
	SPI_55S	SPI	SPI_ALT_MOSI	47
	SPI_55S	SPI	SPI_ALT_MISO	47
	SPI_55S	SPI	SPI_ALT_CLK	47
	HDA_55S	HDA	HDA_BIT_CLK	18 55
	HDA_55S	HDA	HDA_BIT_CLK_R	18
	HDA_55S	HDA	HDA_RST_L	18 55
	HDA_55S	HDA	HDA_RST_R_L	18
	HDA_55S	HDA	HDA_SDOUT	18 55
	HDA_55S	HDA	HDA_SDOUT_R	18
	HDA_55S	HDA	HDA_SYNC	18 55
	HDA_55S	HDA	HDA_SYNC_R	18
	HDA_55S	HDA	HDA_SDIN0	18 55
	HDA_55S	HDA	AUD_SDI_R	55
		HDA	AUD_SPDIF_IN	59 81
		HDA	AUD_SPDIF_OUT	55 59
		HDA	AUD_SPDIF_CHIP	55
	HDA_55S	HDA	AUD_SPKR_OUTLO1L_NOUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO1L_POUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO1R_NOUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO1R_POUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2L_NOUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2L_POUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2R_NOUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2R_POUT	58 59 92
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT	18 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN	18 27
	PCH_55S	COMP_PCH	PCH_USB_RBIAS	20
	PCH_55S	COMP_PCH	PCH_SATAICOMP	18
	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP	18
	PCH_55S	COMP_PCH	PCH_DMI_COMP	19
	CLK_XTAL	XTAL	USB_HUB1_XTAL1	34
	CLK_XTAL	XTAL	USB_HUB1_XTAL2	34
	PCH_55S	COMP_PCH	USB_HUB1_RBIAS	34
	CLK_XTAL	XTAL	USB_HUB2_XTAL1	35
	CLK_XTAL	XTAL	USB_HUB2_XTAL2	35
	PCH_55S	COMP_PCH	USB_HUB2_RBIAS	35

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IBEX PEAK CONSTRAINTS

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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

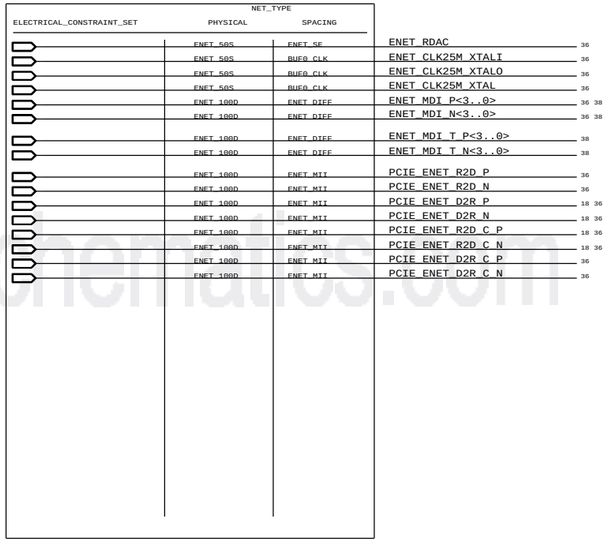
SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?

SOURCE: BROADCOM 5764-DS04-RDS. PAGE 38



FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

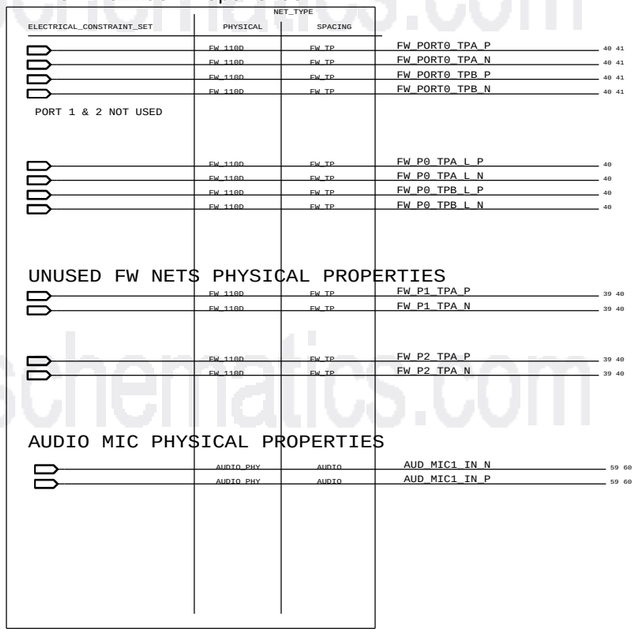
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_PHY	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=STANDARD	?

FireWire Net Properties



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2016

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ENET/FIREWIRE CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
ASSINGED IN CONT. MGR.			
	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0> 80
	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0> 80
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_P<3..0> 77
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_N<3..0> 77
	DP_85D	DISPLAYPORT	DP_INT_LINK_P<3..0> 77 79
	DP_85D	DISPLAYPORT	DP_INT_LINK_N<3..0> 77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_P 77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_N 77 79
	DP_85D	DISPLAYPORT	DP_EXT_LINK_P<3..0> 78 80
	DP_85D	DISPLAYPORT	DP_EXT_LINK_N<3..0> 78 80
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_P 78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_N 78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_P<3..0> 78
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_N<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_P<3..0> 73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_N<3..0> 73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_P 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_N 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_P 73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_N 73 78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0> 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0> 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_P 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_N 79
	DP_85D	DISPLAYPORT	DP_MUX_P<3..0> 78 79
	DP_85D	DISPLAYPORT	DP_MUX_N<3..0> 78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_P 78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_N 78 79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_P 79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_N 79
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_P<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_N<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_P<3..0> 79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_N<3..0> 79
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_P 78
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_N 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_P<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_N<3..0> 78

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P 73 76
	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N 73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P 73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N 73 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N 74 76
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0> 73 76
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0> 73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0> 73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0> 73 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0> 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0> 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0> 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0> 74 76

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GRAPHICS CONSTRAINTS

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	48
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	48
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	48
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	48
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	48
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	48
	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	48
	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	48
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	48 88
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	48 88
I130	SMB_5SS	SMB	SMBUS_PCH_S0_CLK	48
I131	SMB_5SS	SMB	SMBUS_PCH_S0_DATA	48
I160	SMB_5SS	SMB	SMBUS_PCH_CLK	18 48
I161	SMB_5SS	SMB	SMBUS_PCH_DATA	18 48
I137	SMB_5SS	SMB	SML_PCH_0_CLK	18 48
I138	SMB_5SS	SMB	SML_PCH_0_DATA	18 48
I139	SMB_5SS	SMB	SML_PCH_1_CLK	18 48
I140	SMB_5SS	SMB	SML_PCH_1_DATA	18 48
I197	CLK_XTAL	XTAL	SMC_EXTAL	45 46
I196	CLK_XTAL	XTAL	SMC_XTAL	45 46

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
I87	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
I88	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
I89	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	51
I90	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	51
I200	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
I201	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
I93	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	51
I94	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	51
I101	THERM_DIFF	THERMAL	SNS_LCD_P	51 92
I102	THERM_DIFF	THERMAL	SNS_LCD_N	51 92
I103	THERM_DIFF	THERMAL	SNS_ODD_P	51 92
I104	THERM_DIFF	THERMAL	SNS_ODD_N	51 92
I105	THERM_DIFF	THERMAL	SNS_CPU_H_P	51
I106	THERM_DIFF	THERMAL	SNS_CPU_H_N	51
I107	THERM_DIFF	THERMAL	SNS_SKIN_P	51 92
I108	THERM_DIFF	THERMAL	SNS_SKIN_N	51 92
I109	THERM_DIFF	THERMAL	SNS_AMB_P	51 92
I110	THERM_DIFF	THERMAL	SNS_AMB_N	51 92
I111	THERM_DIFF	THERMAL	SNS_MXM_P	51
I112	THERM_DIFF	THERMAL	SNS_MXM_N	51
I192	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 51
I193	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 51
I115		THERMAL	HDD_OOB_TEMP_FILT	51 92
I133		THERMAL	HDD_OOB_TEMP	51
I134		THERMAL	HDD_OOB_TEMP_R	51
I132		THERMAL	SMC_HDD_OOB_TEMP	51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
I67	THERM_DIFF	THERMAL	MXM_ISENSE_P	50
I68	THERM_DIFF	THERMAL	MXM_ISENSE_N	50
I69	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_P	49
I180	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_N	49
I148	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_P	49
I149	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_N	49
I150	THERM_DIFF	THERMAL	SENSE_CPU_1V5_P	49
I151	THERM_DIFF	THERMAL	SENSE_CPU_1V5_N	49
I152	THERM_DIFF	THERMAL	SENSE_CPU_VTT_P	49
I153	THERM_DIFF	THERMAL	SENSE_CPU_VTT_N	49
I181	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_P	
I182	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_N	
I183	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_P	
I184	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_N	
I185		THERMAL	GND_SMC_AVSS	45 46 49 50
I154		THERMAL	SMC_CPU_1V5_ISENSE	46 49
I155		THERMAL	SMC_CPU_1V5_ISENSE_R	49
I156		THERMAL	SMC_CPU_1V5_VSENSE	46 49
I172		THERMAL	SMC_CPU_VTT_ISENSE	46 49
I163		THERMAL	SMC_CPU_VTT_ISENSE_R	49
I164		THERMAL	SMC_CPU_VTT_VSENSE	46 49
I165		THERMAL	SMC_CPU_1V8_ISENSE	46 49
I166		THERMAL	SMC_CPU_1V8_ISENSE_R	
I167		THERMAL	SMC_CPU_1V8_VSENSE	46 49
I168		THERMAL	SMC_CPU_VSENSE	45 49
I128	VID_PHY	VR_CTL	VR_CPU_IOUT	13 64
I131	THERM_DIFF	THERMAL	VR_ISNS_CPU_P	49
I130	THERM_DIFF	THERMAL	VR_ISNS_CPU_N	49
I129		THERMAL	SNS_PS_CPU_ISNS	49
I114		THERMAL	SMC_CPU_ISENSE	45 49
I169		THERMAL	SMC_CPU_INPUT_ISENSE	46
I171		THERMAL	SMC_CPU_INPUT_VSENSE	46
I172		THERMAL	SMC_DIMM_1V5_ISENSE	46 50
I173		THERMAL	SMC_1V5_S3_ISENSE_R	
I174		THERMAL	SMC_DIMM_1V5_VSENSE	46 50
I177		THERMAL	SMC_GPU_ISENSE	45 50
I178		THERMAL	SMC_MXM_ISENSE_R	50
I188		THERMAL	SMC_GPU_VSENSE	45 50

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING	VOLTAGE		
H128	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1	65
H129	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2	65
H130	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3	65
H131	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE4	66
H132	POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE	69
H133	POWER	SWITCHNODE	5V	P5VS3_REG_PHASE	69
H134	POWER	SWITCHNODE	1.1V	VTT_REG_PHASE1	67
H135	POWER	SWITCHNODE	1.1V	VTT_REG_PHASE2	67
H139	POWER	SWITCHNODE	3.4V	P3V42G3H_SW	71
H138	POWER	SWITCHNODE	1.05V	PCHCORE_REG_PHASE	68
H137					
H141	POWER	SWITCHNODE	1.05V	P1V05_S5_REG_PHASE	71
H139	POWER	SWITCHNODE	1.5V	DDR_REG_PHASE	70
H140	POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE	70
H143	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_A	28 30
H142	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_B	28 31
H144	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_A	28 30
H147	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_B	28 31
H68	POWER	POWER	12V	PP12V_S0_CPUVTT_FLTD	
H148	POWER	POWER	12V	PP12V_AUD_SPKRAMP_PLANE	57 58 60
H149	POWER	POWER	12V	PP12V_LCD	77
H150	POWER	POWER	12V	PP12V_LCD_CONN	77
H151	POWER	POWER	12V	PP12V_S0	6 63
H154	POWER	POWER	12V	PP12V_S0_CPU_FLTRD	64 65 66
H153	POWER	POWER	12V	PP12V_S0_FAN0_L	52 92
H175	POWER	POWER	12V	PP12V_S0_FAN1_L	52 92
H176	POWER	POWER	12V	PP12V_S0_FAN2_L	53 92
H69	POWER	POWER	12V	PP12V_G3H	6 71
H69	POWER	POWER	12V	PP12V_G3H_R	71
H70	POWER	POWER	12V	PP12V_S5	6
H155	POWER	POWER	12V	P12V_S0_FW	
H27	POWER	POWER	12V	P12V_S0_FW_CL	
H27	POWER	POWER	12V	P12V_S0_FW_D	
H26	POWER	POWER	12V	P12V_S0_FW_R	
H25	POWER	POWER	12V	FW_PORT0_VP	41
H27	POWER	POWER	12V	FW_PORT0_VP_F	41
H44	POWER	POWER	12V	PPVP_FW_PHY_CPS	40 41
H49	POWER	POWER	12V	PP12V_S3	6
H55	POWER	POWER	12V	PP12V_S3_WM_FLT	44
H129	POWER	POWER	1.1V	PPVCORE_S0_CPU	6
H258	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1	65
H262	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2	65
H263	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3	65
H265	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG4	66
H256	POWER	POWER	1.05V	PP1V05_SM_SOURCE	72
H174	POWER	POWER	1.05V	PP1V05_S0	6
H175	POWER	POWER	1.05V	PP1V05_S0_CK505_F	26
H178	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA	17 22
H181	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	
H180	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB	17 22
H181	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	
H182	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP	22 24
H183	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_FDI	22 24
H184	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA	22 24
H185	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK	22 24
H186	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK_F	24
H187	POWER	POWER	1.05V	PP1V05_S0_CIO_VDD1P0_DP	
H189	POWER	POWER	1.05V	PP1V05_S0_CIO_VDD1P0_DP_PLL	
H190					
H614	POWER	POWER	1.05V	PP1V05_SM_PCH_LAN	6
H152	POWER	POWER	1.05V	PP1V05_S5	6
H57	POWER	POWER	1.05V	PP1V05_SM	6
H260	POWER	POWER	1.1V	PPVTT_S0	6
H55	POWER	POWER	1.1V	PPVTT_S0_CPU	6 49
H268	POWER	POWER	0.75V	PPVTT_S0_DDR	6
H61	POWER	POWER	0.75V	PP0V75_S0	6
H190	POWER	POWER	1.2V	PP1V2_S5_ENET	37
H190	POWER	POWER	1.5V	PP1V5_S0	6
H190	POWER	POWER	1.5V	PP1V5_S0_CK505_F	26
H187	POWER	POWER	1.5V	PP1V5_S0_CK505_R	26
H190	POWER	POWER	1.5V	PP1V5_S3	6
H67	POWER	POWER	1.5V	PP1V5_CPU_MEM	6 49
H200	POWER	POWER	1.5V	PP1V8R1V5_S0_PCH_VCCVRM	22 24
H150	POWER	POWER	1.5V	PP1V5_FW_VDDA	39
H205	POWER	POWER	1.5V	PP1V8_S0	6
H205	POWER	POWER	1.8V	PP1V8_S0_CPU	6 49
H206	POWER	POWER	1.96V	PP1V96_FW_PLLVDD	39
H206	POWER	POWER	1.96V	PP1V95_FW_FWPHY	39 40

POWER NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING	VOLTAGE		
H618	POWER	POWER	3.3V	PP3V3_S0	6
H619	POWER	POWER	3.3V	PP3V3_S0_CK505_F	26
H247	POWER	POWER	3.3V	PP3V3_S0_DPAUX	80
H245	POWER	POWER	3.3V	PP3V3_S0_DPFUSE	80
H246	POWER	POWER	3.3V	PP3V3_S0_DPPWR	80
H223	POWER	POWER	3.3V	PP3V3_S0_HS_F	61
H676	POWER	POWER	3.3V	PP3V3_S0M	6
H677	POWER	POWER	3.3V	PP3V3_MINI	33
H612	POWER	POWER	3.3V	PP3V3_ENET	36 37
H223	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC	17 22
H696	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	
H695	POWER	POWER	3.3V	PP3V3_S0_TSENS_R	51
H242	POWER	POWER	3.3V	PP3V3_S3	6 92
H657	POWER	POWER	3.3V	PP3V3_S3_BT_FLT	44
H246	POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT	44
H658	POWER	POWER	3.3V	PP3V3_S3_WM_FLT	44
H238	POWER	POWER	3.3V	PP3V3_S5	6
H277	POWER	POWER	3.3V	PPVTT_S3_DDR_BUF	70
H278	POWER	POWER	3.3V	PPV_S0_MXM_PWRSRC	50
H240	POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST	22
H240	POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUS	22
H660	POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUSBYP	22
H262	POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC	22
H618	POWER	POWER	3.3V	PPVOUT_S0_PCH_VCCRTC_NCTF	
H667	POWER	POWER	3.3V	PPVBATT_G3_RTC	27
H266	POWER	POWER	3.3V	PPVBATT_G3_RTC_R	27
H697	POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK	59
H698	POWER	POWER	3.3V	PP3V3_FW_AVDD	39
H241	POWER	POWER	3.3V	PP3V3_FW_ESD	41
H243	POWER	POWER	3.3V	PP3V3_FW_PLLVDD	39
H240	POWER	POWER	3.3V	PP3V3_FW_VDDA	39
H215	POWER	POWER	3.3V	PP3V3_G3_RTC	18 22 24 27
H214	POWER	POWER	3.3V	PP_ENET_CTRL12	37
H230	POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC	45
H233	POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC	45 46
H666	POWER	POWER	3.42V	PP3V42_G3H	6
H669	POWER	POWER	3.42V	PP3V42_G3H_R	71
H672	POWER	POWER	4.5V	4V5_REG_IN	55
H238	POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG	55
H237	POWER	POWER	5V	PP5V_S0	6 92
H238	POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC	64
H238	POWER	POWER	5V	PP5V_S0_PCH_V5REF	22 24
H669	POWER	POWER	5V	PP5V_S0_SATA_FET	42
H245	POWER	POWER	5V	PP5V_S3	6
H242	POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT	70
H658	POWER	POWER	5V	PP5V_S3_CAMERA_FLT	44
H658	POWER	POWER	5V	PP5V_S3_IR_FLT	44
H400	POWER	POWER	5V	VREFMARGIN_DIMMA_P5V	28
H400	POWER	POWER	5V	VREFMARGIN_DIMMB_P5V	28
H240	POWER	POWER	5V	PP5V_S5	6
H240	POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS	22 24
H688	POWER	POWER	5V	PP5V_CPUVTT_VR	67
H247	POWER	POWER	5V	PP5V_USB2_PORT0	43
H250	POWER	POWER	5V	PP5V_USB2_PORT0_F	43
H248	POWER	POWER	5V	PP5V_USB2_PORT1	43
H249	POWER	POWER	5V	PP5V_USB2_PORT1_F	43
H252	POWER	POWER	5V	PP5V_USB2_PORT2	43
H253	POWER	POWER	5V	PP5V_USB2_PORT2_F	43
H254	POWER	POWER	5V	PP5V_USB2_PORT3	43
H255	POWER	POWER	5V	PP5V_USB2_PORT3_F	43
H640	POWER	POWER		DDR_REG_PGND	70
H640	POWER	POWER		DDR_REG_CSGND	70

SENSING NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
H156	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	64 65
H156	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	64 65
H157	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	64
H158	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	64
H160	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	64 65
H159	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	64 65
H161	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	64
H162	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	64
H163	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	64 65
H164	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	64 65
H165	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	64
H166	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	64
H167	SNS_DIFF	THERMAL	VR_CPU_ISNS4_P	64 66
H168	SNS_DIFF	THERMAL	VR_CPU_ISNS4_N	64 66
H169	SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_P	64
H170	SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_N	64
H659	SNS_DIFF	THERMAL	VR_CPU_ISNS1_XW_P	65
H660	SNS_DIFF	THERMAL	VR_CPU_ISNS1_XW_N	65
H661	SNS_DIFF	THERMAL	VR_CPU_ISNS2_XW_P	65
H662	SNS_DIFF	THERMAL	VR_CPU_ISNS2_XW_N	65
H663	SNS_DIFF	THERMAL	VR_CPU_ISNS3_XW_P	65
H664	SNS_DIFF	THERMAL	VR_CPU_ISNS3_XW_N	65
H665	SNS_DIFF	THERMAL	VR_CPU_ISNS4_XW_P	66
H666	SNS_DIFF	THERMAL	VR_CPU_ISNS4_XW_N	66
H670	SNS_DIFF		CPU_VCC_PKG_SENSE_P	13 49 64
H670	SNS_DIFF		CPU_VCC_PKG_SENSE_N	13 64
H56	SNS_DIFF		CPU_VTTSENSE_P	13 49 67
H67	SNS_DIFF		CPU_VTTSENSE_N	13 67
H197	SNS_DIFF		CPU_VTTSENSE_R_P	67
H197	SNS_DIFF		CPU_VTTSENSE_R_N	67
H58	SNS_DIFF		VR_CPU_VSEN	64
H59	SNS_DIFF		VR_CPU_RGND	64
H140	SNS_DIFF		VR_CPU_VSNS_R_N	64
H192	SNS_DIFF		VR_CPU_VSNS_R_P	64
H145	SNS_DIFF		VR_CPU_VSNS_XW_P	64
H150	SNS_DIFF		VR_CPU_VSNS_XW_N	64

VR CTRL NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
H727	VR_CTL_PHY	VR_CTL	VR_CPU_PH1_SNUB	65
H728	VR_CTL_PHY	VR_CTL	VR_CPU_PH2_SNUB	65
H729	VR_CTL_PHY	VR_CTL	VR_CPU_PH3_SNUB	65
H730	VR_CTL_PHY	VR_CTL	VR_CPU_PH4_SNUB	66
H731	VR_CTL_PHY	VR_CTL	VR_CPU_PWM1	64 65
H732	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2	64 65
H733	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R	64
H734	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3	64 65
H735	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R	64
H736	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4	64 66
H737	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R	64
H738	VR_CTL_PHY	VR_CTL	VR_CPU_REF	64
H739	VR_CTL_PHY	VR_CTL	VR_CPU_SS	64
H740	VR_CTL_PHY	VR_CTL	VR_CPU_TCOMP	64
H741	VR_CTL_PHY	VR_CTL	VR_CPU_TM	64
H742	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT1_RC	65
H743	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT2_RC	65
H744	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT3_RC	65
H745	VR_CTL_PHY	VR_CTL	VR_CPU_COMP	64
H746	VR_CTL_PHY	VR_CTL	VR_CPU_COMP_R	64
H747	VR_CTL_PHY	VR_CTL	VR_CPU_COMP_RC	64
H748	VR_CTL_PHY	VR_CTL	VR_CPU_DAC	64
H749	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_BOOT	65
H750	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL	65
H751	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_LGATE	65
H752	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_UGATE	65
H753	VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_BOOT	65
H754	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_GDSEL	65
H755	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_LGATE	65
H756	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_UGATE	65
H757	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_BOOT	65
H758	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL	65
H759	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_LGATE	65
H760	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_UGATE	65
H761	VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_BOOT	66
H762	VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_GDSEL	66
H763	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV4_LGATE	66
H764	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV4_UGATE	66
H767	VR_CTL_PHY	VR_CTL	VR_CPU_FAN	64
H768	VR_CTL_PHY	VR_CTL	VR_CPU_FB	64
H769	VR_CTL_PHY	VR_CTL	VR_CPU_FB_R	64
H770	VR_CTL_PHY	VR_CTL	VR_CPU_FS	64
H771	VR_CTL_PHY	VR_CTL	VR_CPU_IMON	49 64
H772	VR_CTL_PHY	VR_CTL	VR_CPU_IOUT_PD	64
H773	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_UGATE	68
H774	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_LGATE	68
H775	VR_CTL_PHY	VR_CTL	PCHCORE_REG_VFB	68
H776	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TON	68
H777	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TRIP	68
H778	VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT	68
H624	VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT_R	68
H401	VR_CTL_PHY	VR_CTL	VTT_REG_BOOT1	67
H402	VR_CTL_PHY	VR_CTL	VTT_REG_BOOT2	67
H403	VR_CTL_PHY	VR_CTL	VTT_REG_COMP	67
H404	VR_CTL_PHY	VR_CTL	VTT_REG_FB	67
H405	VR_CTL_PHY	VR_CTL	VTT_REG_FS	67
H406	VR_CTL_PHY	VR_CTL	VTT_REG_ICOMP	67
H407	VR_CTL_PHY	VR_CTL	VTT_REG_IREF	67
H408	VR_CTL_PHY	VR_CTL	VTT_REG_ISUM	67
H409	VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE1	67
H410	VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE2	67
H411	VR_CTL_PHY	VR_CTL	VTT_REG_OCSET	67
H412	VR_CTL_PHY	VR_CTL	VTT_OFST	67
H413	VR_CTL_PHY	VR_CTL	VTT_REG_REF	67
H414	VR_CTL_PHY	VR_CTL	VTT_REG_RGND	67
H415	VR_CTL_PHY	VR_CTL	VTT_SEL	67
H416	VR_CTL_PHY	VR_CTL	VTT_REG_UGATE2	67
H417	VR_CTL_PHY	VR_CTL	VTT_REG_UGATE1	67
H418	VR_CTL_PHY	VR_CTL	VTT_REG_PH1_SNUB	67
H419	VR_CTL_PHY	VR_CTL	VTT_REG_PH2_SNUB	67
H420	VR_CTL_PHY	VR_CTL	VTT_REG_VSEN	67
H109	VR_CTL_PHY	VR_CTL	P1V05S5_REG_VFB	71
H660	VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST	71
H660	VR_CTL_PHY	VR_CTL	P3V42G3H_FB	71

VR CTRL NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
H437	VR_CTL_PHY	VR_CTL	DDR_REG_CS	70
H438	VR_CTL_PHY	VR_CTL	DDR_REG_FB	70
H439	VR_CTL_PHY	SWITCHNODE	DDR_REG_LGATE	70
H440	VR_CTL_PHY	SWITCHNODE	DDR_REG_UGATE	70
H441	VR_CTL_PHY	VR_CTL	DDR_REG_BOOT	70
H442	VR_CTL_PHY	VR_CTL	DDR_REG_BOOT_R	70
H443	VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS	70
H444	VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS	70
H445	VR_CTL_PHY	VR_CTL	P1V8_REG_POR	70
H446	VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT	69
H447	VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT_R	69
H448	VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB	69
H449	VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN	69
H450	VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_LGATE	69
H451	VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET	69
H452	VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_UGATE	69
H453	VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB	69
H454	VR_CTL_PHY	VR_CTL	P5VS3_REG_BOOT	69
H455	VR_CTL_PHY	VR_CTL	P5VS3_REG_FB	69
H462	VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN	69
H463	VR_CTL_PHY	SWITCHNODE	P5VS3_REG_LGATE	69
H464	VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET	69
H466	VR_CTL_PHY	SWITCHNODE	P5VS3_REG_UGATE	69

VR VID NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
H499	VID_PHY	VR_CTL	CPU_VID<0>	13 16 64
H492	VID_PHY	VR_CTL	CPU_VID<1>	13 16 64
H521	VID_PHY	VR_CTL	CPU_VID<2>	13 16 64
H522	VID_PHY	VR_CTL	CPU_VID<3>	13 16 64
H523	VID_PHY	VR_CTL	CPU_VID<4>	13 16 64
H524	VID_PHY	VR_CTL	CPU_VID<5>	13 16 64
H525	VID_PHY	VR_CTL	CPU_VID<6>	13 16 64
H526	VID_PHY	VR_CTL	CPU_VID<7>	13 16 64
H155	VID_PHY	VR_CTL	CPU_PSI_L	13 16 64

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	39_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.2MM	?

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POWER CONSTRAINTS

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

	NET_TYPE PHYSICAL	SPACING		
T2	PM		PLT_RESET_L	20 27
T4	PM_VTT		PLT_RESET_LS1V1_L	11
T5	PM		PM_ACDC_PS_ON	6
T8	PM		PM_BATLOW_L	15 19 45
T9	PM		PM_CLK32K_SUSCLK	9 45 85
T10	PM		PM_CLK32K_SUSCLK_R	9 19 85
T11	PM		PM_CLKRUN_L	15 19 45 47
T6				
T13	PM		PM_EXT_TS_L<0>	11 46
T6	PM		PM_EXT_TS_L<1>	11 46
T12	PM		PM_LAN_PWRGD	15 19
T117	PM_VTT		FSB_CPURSTOUT_L	11 25
T120	PM		USB_HUB_RESET_L	34 35
T25	PM_VTT		PM_MEM_PWRGD	11 19
T24	PM		PM_ME_PWRGD	19 63
T27	PM		PM_ME_S0_EN_G	72
T26	PM		PM_ME_S0_EN_G1	72
T28	PM		PM_ME_S0_EN_R	72
T38	PM		PM_MXM_PGOOD	63 74
T29	PM		PM_PCH_PWRGD	19 63
T31	PM		PM_PGOOD_DDRREG_S3	5 62 70
T33	PM		PM_PGOOD_PVCORE_CPU	5 26 63 64
T32	PM		PM_PWRBTN_L	19 25 45
T35	PM		PM_RSMRST_L	45 62
T34	PM		PM_RSMRST_PCH_L	19 62
T36	PM		PM_SLP_M_L	5 19 62
T38	PM		PM_SLP_M_R	
T37	PM		PM_SLP_S3_L	5 19 32 33 37 46 62 63
T40	PM		PM_SLP_S3_L_AND_S0_RDY	
T139	PM		PM_SLP_S4_1_L	19 62
T119	PM		PM_SLP_S4_2_L	19 45 46
T118	PM		PM_SLP_S4_3_L	5 19
T39	PM		PM_SLP_S4_L	19 32
T43	PM		PM_SLP_S5_L	19 45
T45	PM		PM_SUS_PWR_ACK	19
T42	PM_VTT		PM_SYNC	11 19
T122	PM		SDCARD_PLT_RST_L	27 44
T46	PM		PM_SYSRST_L	19 27 45
T44	PM		PM_SYS_PWRGD	19 32 63
T48	PM_VTT		PM_THRMTRIP_L	11 21 46
T48	PM		RSMRST_PWRGD	45 63
T47	PM		RTC_RESET_L	18 91
T50	PM_VTT		CPU_PWRGD	11 21 25
T49	PM		CPU_RESET_L	11 27
T54	PM		PGOOD_1V05ME_G1	63
T57	PM		PGOOD_1V05ME_G2	63
T56	PM		PGOOD_1V8_S0_G1	63
T52	PM		PGOOD_1V8_S0_G2	63
T53	PM		PGOOD_CPU_GFX_DDR	63
T55	PM		PGOOD_P12V_S3	
T55	PM		PGOOD_P1V05_ME_S5	
T58	PM		PGOOD_P1V5_S0	72
T59	PM		PGOOD_P1V8_S0	63
T67	PM		PGOOD_P3V3_ME	72
T60	PM		PGOOD_P3V3_S0	48 63 72
T63	PM		PGOOD_P3V3_S3	34 72
T62	PM		PGOOD_P5V_S0	62 72
T64	PM		PGOOD_PCH_AND_P1V8	63
T66	PM		PGOOD_PCH_S0	63
T65	PM		PGOOD_SYSPWROK	63
T67	PM		PGOOD_SYSPWROK_R	63
T68	PM		RTC_RESET_L	18 91
T69	PM		P12V_S3_EN	62 72
T71	PM		P1V05_ME_SM_EN	62 72
T70	PM		P1V5_S0_EN	62 72
T72	PM		P3V3ME_EN	62 72
T74	PM		P3V3S0_EN	62 72
T73	PM		P3V3S3_EN	62 72
T76	PM		P5VS0_EN	62 72
T75	PM		P5VS3_EN	62 69
T77	PM		PCHCORE_REG_EN	62 68
T78	PM		PCHCORE_REG_PGOOD	5 62 63 68
T79	PM		PEG_RESET_L	9 27
T80	PM		SDCARD_RESET	21 25 44 92

	NET_TYPE PHYSICAL	SPACING		
T82	PM		4V5_REG_EN	55
T81	PM		ALL_SYS_PWRGD_R	6 25 32 63
T84	PM		ALL_SYS_PWRGD_SMC	45 63
T83	PM		CK505_27MHZ_EN	26
T85	PM		CPUVTT_REG_EN	62 67
T86	PM_VTT		CPUVTT_REG_PGOOD	11 62 63 67
T87	PM		CPU_MEM_RESET_L	11 32
T88	PM		DDRVTT_EN	32 62 70
T89	PM		DEBUG_RESET_L	27 47
T90	PM		FWPHY_RESET_L	39
T91	PM		FWXIO_SNOOP_EN	39
T92	PM		FW_RESET_L	27 39
T93	PM		GFX_VR_EN	
T94	PM		GFX_VR_PGOOD	
T95	PM		LAN_RESET_L	27 36
T97	PM		MEM_RESET_L	30 31 32
T98	PM		MINI_RESET_L	27 33
T99	PM		SMC_DELAYED_PWRGD	46 63
T100	PM		SMC_LRESET_L	27 45
T101	PM		SMC_RESET_L	45 46 47
T102	PM		T28_RESET_L	
T103	PM_VTT		XDP_CPUPWRGD	11 25
T104	PM_VTT		XDP_DBRESET_L	11 25 27
T105	PM_VTT		XDP_PWRGD	25

NET PHYSICAL FOR NC NETS
REMOVE WHEN CHECKPLUS IS FIXED

	NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	PCIE GRAPHICS			
T106		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_N
T108		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_P
T107		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_N
T109		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_P
T110		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_N
T111		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_P
T112	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_N
T113	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_P
T114	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_N
T115	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_P
T116	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_N
T117	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_P

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PM RESETS ENABLES PGOOD CONST

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

- IN PP5V_S3_CAMERA — FUNC_TEST=TRUE, MIN_ALLOWED_TPS=1
- 85 44 IN USB_CAMERA_L_P — FUNC_TEST=TRUE
- 85 44 IN USB_CAMERA_L_N — FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

- 85 44 IN USB_SDCARD_L_P — FUNC_TEST=TRUF
- 85 44 IN USB_SDCARD_L_N — FUNC_TEST=TRUF
- 91 44 25 21 IN SDCARD_RESET — FUNC_TEST=TRUF

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

- 85 44 IN USB_BT_L_P — FUNC_TEST=TRUF
- 85 44 IN USB_BT_L_N — FUNC_TEST=TRUF

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

- 85 44 IN USB_IR_L_P — FUNC_TEST=TRUF
- 85 44 IN USB_IR_L_N — FUNC_TEST=TRUF

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

- 84 42 IN SATA_ODD_R2D_P — FUNC_TEST=TRUF
- 84 42 IN SATA_ODD_R2D_N — FUNC_TEST=TRUF
- 84 42 IN SATA_ODD_D2R_C_N — FUNC_TEST=TRUF
- 84 42 IN SATA_ODD_D2R_C_P — FUNC_TEST=TRUF
- 45 42 IN SMC_ODD_DETECT — FUNC_TEST=TRUF

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

- 84 42 IN SATA_HDD_R2D_P — FUNC_TEST=TRUF
- 84 42 IN SATA_HDD_R2D_N — FUNC_TEST=TRUF
- 84 42 IN SATA_HDD_D2R_C_N — FUNC_TEST=TRUF
- 84 42 IN SATA_HDD_D2R_C_P — FUNC_TEST=TRUF

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

- 88 51 IN SNS_LCD_P — FUNC_TEST=TRUF
- 88 51 IN SNS_LCD_N — FUNC_TEST=TRUF

J5521 AMBIENT TEMP SENSOR

- 88 51 IN SNS_AMB_P — FUNC_TEST=TRUF
- 88 51 IN SNS_AMB_N — FUNC_TEST=TRUF

J5551 ODD TEMP SENSOR

- 88 51 IN SNS_ODD_P — FUNC_TEST=TRUF
- 88 51 IN SNS_ODD_N — FUNC_TEST=TRUF

J5600 ODD FAN

- 52 IN FAN_0_PWR_L — FUNC_TEST=TRUF
- 52 IN FAN_TACH0_L — FUNC_TEST=TRUF
- 89 52 IN PP12V_S0_FAN0_L — FUNC_TEST=TRUF
- 52 IN FAN_0_GND — FUNC_TEST=TRUF

J5700 CPU FAN

- 53 IN FAN_2_PWR_L — FUNC_TEST=TRUF
- 53 IN FAN_TACH2_L — FUNC_TEST=TRUF
- 89 53 IN PP12V_S0_FAN2_L — FUNC_TEST=TRUF
- 53 IN FAN_2_GND — FUNC_TEST=TRUF

J5601 HD FAN

- 52 IN FAN_1_PWR_L — FUNC_TEST=TRUF
- 52 IN FAN_TACH1_L — FUNC_TEST=TRUF
- 89 52 IN PP12V_S0_FAN1_L — FUNC_TEST=TRUF
- 52 IN FAN_1_GND — FUNC_TEST=TRUF

J5550 HDD TEMP SENSOR

- 88 51 IN HDD_OOB_TEMP_FILT — FUNC_TEST=TRUF

J5560 SKIN TEMP SENSOR

- 88 51 IN SNS_SKIN_P — FUNC_TEST=TRUF
- 88 51 IN SNS_SKIN_N — FUNC_TEST=TRUF

J6601 AUDIO MICROPHONE

- 59 IN AUD_MIC_IN1_N_CONN — FUNC_TEST=TRUF
- 59 IN GND_AUDIO_MIC1_CONN — FUNC_TEST=TRUF
- 59 IN AUD_MIC_IN1_P_CONN — FUNC_TEST=TRUF

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

- 85 59 58 IN AUD_SPKR_OUTLO2R_POUT — FUNC_TEST=TRUF
- 85 59 58 IN AUD_SPKR_OUTLO2R_NOUT — FUNC_TEST=TRUF
- 85 59 57 IN AUD_SPKR_OUTLO1R_POUT — FUNC_TEST=TRUF
- 85 59 57 IN AUD_SPKR_OUTLO1R_NOUT — FUNC_TEST=TRUF

J6603 AUDIO LEFT SPEAKER

- 85 59 58 IN AUD_SPKR_OUTLO2L_POUT — FUNC_TEST=TRUF
- 85 59 58 IN AUD_SPKR_OUTLO2L_NOUT — FUNC_TEST=TRUF
- 85 59 57 IN AUD_SPKR_OUTLO1L_POUT — FUNC_TEST=TRUF
- 85 59 57 IN AUD_SPKR_OUTLO1L_NOUT — FUNC_TEST=TRUF

- GND — 16 TP'S — FUNC_TEST=TRUF, MIN_ALLOWED_TPS=16
- 89 6 IN PP3V3_S3 — 2 TP'S — FUNC_TEST=TRUF, MIN_ALLOWED_TPS=2
- 69 6 IN PP5V_S3_REG — 2 TP'S — FUNC_TEST=TRUF, MIN_ALLOWED_TPS=1
- 89 6 IN PP5V_S0 — FUNC_TEST=TRUF, MIN_ALLOWED_TPS=1

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